MX98902A

ETHERNET NETWORK CONTROLLER FOR TWISTED-PAIR

FEATURES

- Compatible with IEEE 802.3 CSMA/CD standard Ethernet, Cheapernet, and Twisted-Pair (10 BASET)
- Two 16-bit DMA channels
- 16-byte internal FIFO with programmable threshold
- Network statistics storage
- 3 levels of loopback
- Independent system and network clocks
- CMOS technology, 84-pin PLCC or 100-pin PQFP package
- NS DP83902 compatible

GENERAL DESCRIPTION

The MX98902 is designed for easy implementation of CSMA/CD local area networks, which include Ethernet (10BASE5), Thin Ethernet (10BASE2), and Twisted-pair Ethernet (10BASE-T). The Media Access Control (MAC) and Encode-Decode (ENDEC) are provided with an AUI interface. The 10BASE-T transceiver functions according to the IEEE 802.3 standards, and the MX98902 10BASE-T transceiver operates in compliance with the IEEE standard.

The MX98902's functional block consists of the receiver, transmitter, collision, heartbeat, loopback, jabber, and link integrity blocks. When combined with equalization resistors, the transceiver transmits or receives filters, and pulse transformers provide physical interface from the MX98902's ENDEC module and the twisted-pair medium.

Manchester encoding and decoding is made possible through the integrated ENDEC module by means of a differential transceiver and phase lock loop decoder at 10 Mbit/sec. Collision detect translator and diagnostic loopback capability are included in this process. Interfacing directly with the transceiver module, the ENDEC module also provides a fully IEEE compliant AUI (Attachment Unit Interface) to connect with other media transceivers.

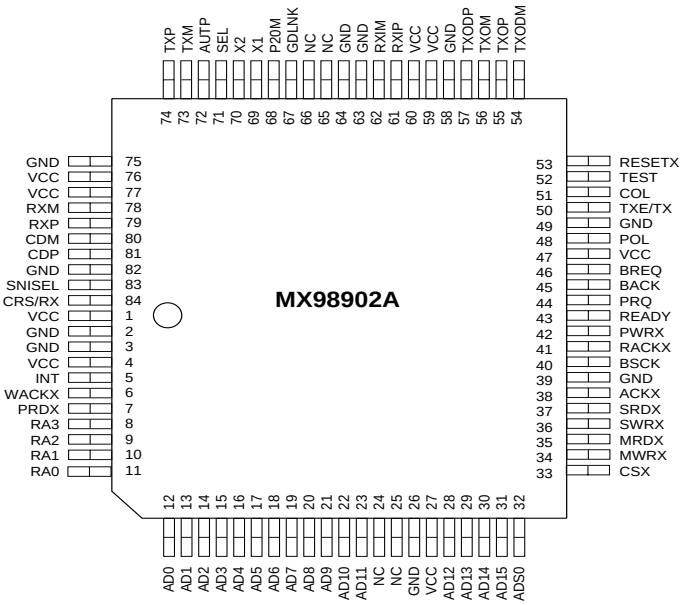
The Media Access Control function, provided by the Ethernet Network Control (ENC) module, effects an efficient packet transmission and reception control through unique dual DMA channels and an internal FIFO. To lessen board cost and area overheads, bus arbitration and memory control logic are integrated.

Designed for easy interface with other transceivers by means of the AUI interface, the MX98902 provides a thorough single chip solution for 10BASE-T IEEE 802.3 network.

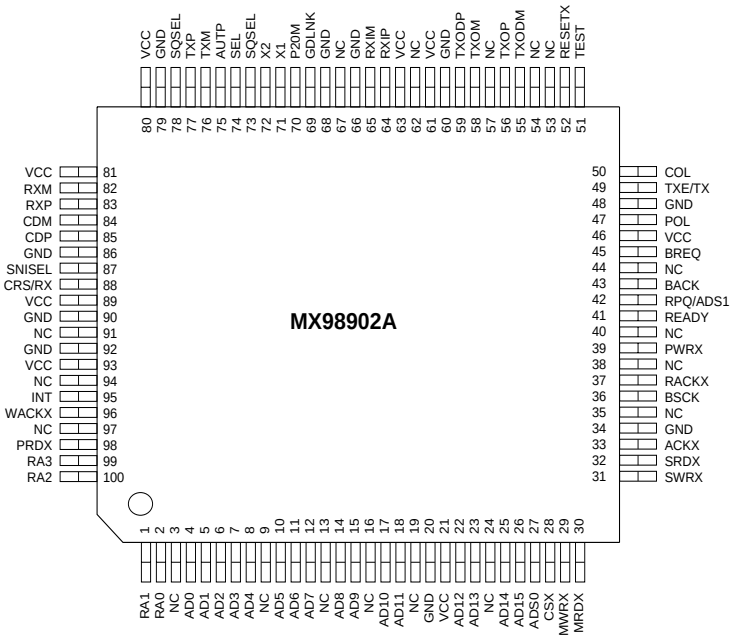
Constraints of CMOS processing require that isolation, whether capacitive or inductive, be used at the AUI differential signal interface for 10BASE5 and 10BASE2 applications.

PIN CONFIGURATIONS

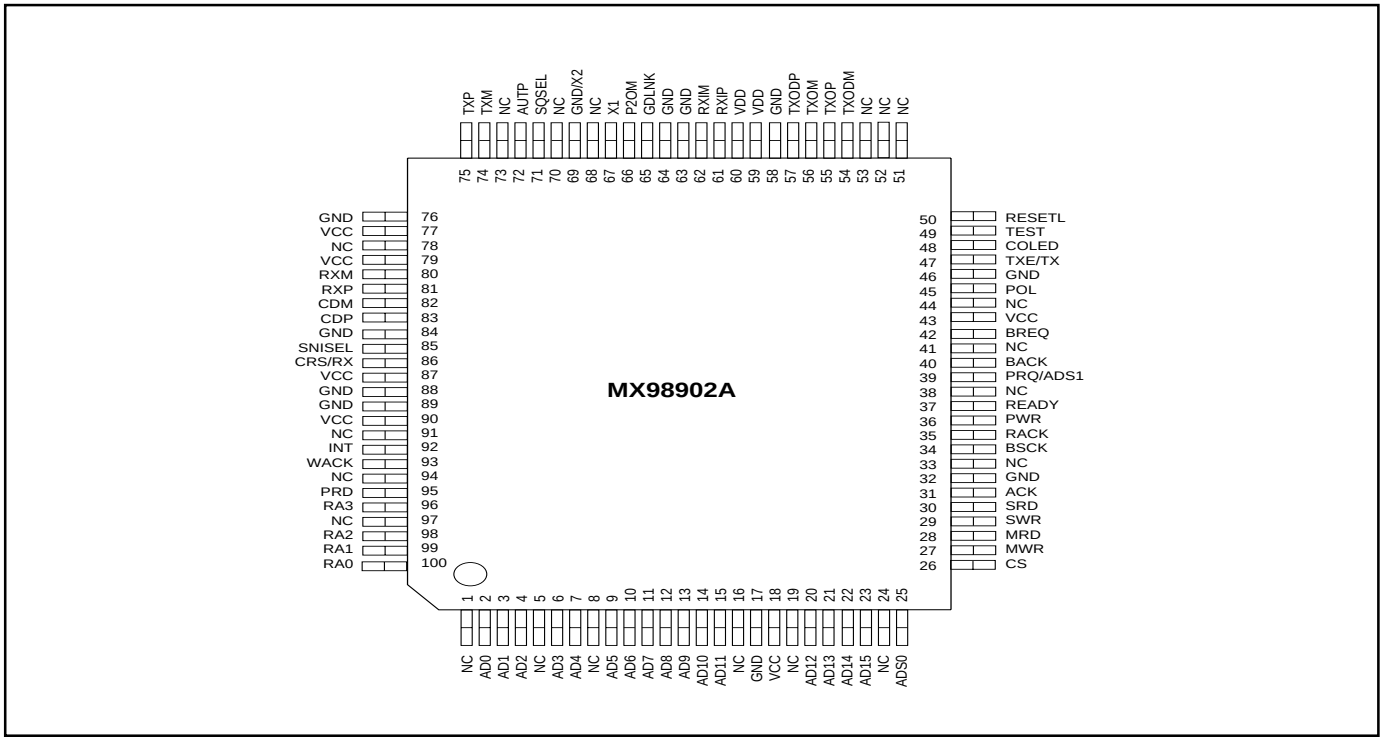
84-PIN PLCC



100-PIN PQFP



100-PIN SQFP


MX98902A
1 NC
2 AD0
3 AD1
4 AD2
5 NC
6 AD3
7 AD4
8 NC
9 AD5
10 AD6
11 AD7
12 AD8
13 AD9
14 AD10
15 AD11
16 NC
17 GND
18 VCC
19 NC
20 AD12
21 AD13
22 AD14
23 AD15
24 NC
25 ADS0
26 CS
27 MWR
28 MRD
29 SWR
30 SRD
31 ACK
32 GND
33 NC
34 BSCK
35 RACK
36 PWR
37 READY
38 NC
39 PRQ/ADS1
40 BACK
41 NC
42 BREQ
43 VCC
44 NC
45 POL
46 GND
47 TXE/TX
48 COLED
49 TEST
50 RESETL
51 NC
52 NC
53 NC
54 TXODM
55 TXOP
56 TXOM
57 TXODP
58 GND
59 VDD
60 VDD
61 RXIP
62 RXIM
63 GND
64 GND
65 GDLNK
66 P2OM
67 X1
68 NC
69 GNDX2
70 NC
71 SQSEL
72 AUTP
73 NC
74 TXM
75 TXP
76 GND
77 VCC
78 NC
79 VCC
80 RXM
81 RXP
82 CDM
83 CDP
84 GND
85 SNISEL
86 CRS/RX
87 VCC
88 GND
89 GND
90 VCC
91 NC
92 INT
93 WACK
94 NC
95 PRD
96 RA3
97 NC
98 RA2
99 RA1
100 RA0

PIN DESCRIPTIONS

A. BUS INTERFACE PINS

SYMBOL	PIN TYPE	PIN NUMBER PQFP	PLCC	SQFP	DESCRIPTION
AD0-AD15	I/O, Z	4-8, 10-12 14,15 17,18 22,23 25,26	12-23 28-31	2-4 6-7 9-15 20-23	**MULTIPLEXED ADDRESS/DATA BUS**: Registeaccess,with DMA inactive, CSX low and ACKX returned fromMX98902, pins AD0-AD7 are used to read/write register data. AD8-AD15 float during I/O transfers. SRDX, SWRX pins are used to select direction of transfer. Bus Master with BACK input asserted. During T1 or memory cycle AD0-AD15 contain address. During T2, T3, T4 AD0-AD15 contain data (word transfer mode). During T2, T3, T4 AD0-AD7 contain data; AD8-AD15 contain address (bytetransfer mode). Direction of transfer is indicated by MX98902 on MWRX, MRDX lines.
ADS0	I/O, Z	27	32	25	**ADDRESS STROBE 0**: Input with DMA inactive and CSX low, latches RA0-RA3 inputs on falling edge. If high, data present on RA0-RA3 will flow through latch. Output when Bus Master latches addresses bits (A0-A15) to external memory during DMA transfers.
CSX	I	28	33	26	**CHIP SELECT**: Chip Select places controller in slave mode for µp access to internal registers. Must be valid through data portion of bus cycle. RA0-RA3 are used to select the internal register. SWRX and SRDX select direction of data transfer.
MWRX	O, Z	29	34	27	**MASTER WRITE STROBE**: Strobe for DMA transfers, active low during write cycles (T2, T3, TW) to buffer memory. Rising edge coincides with the presence of valid output data. TRI-STATE until BACK asserted.
MRDX	O,Z	30	35	28	**MASTER READ STROBE**: Strobe for DMA transfers, active during read cycles (T2, T3, TW) to buffer memory. Input data must be valid on rising edge of MRDX. TRI-STATE until BACK asserted.
SWRX	I	31	36	29	**SLAVE WRITE STROBE**: Strobe from CPU to write an internal register selected by RA0-RA3.
SRDX	I	32	37	30	**SLAVE READ STROBE**: Strobe from CPU to read an internal register selected by RA0-RA3.
ACKX	O	33	38	31	**ACKNOWLEDGE**: Active low when MX98902 grants access to CPU. Used to insert WAIT states to CPU until MX98902 is synchronized for a register read or write operation.
RA0-RA3	I	99,100 1,2	8-11	96 98-100	**REGISTER ADDRESS**: These four pins are used to select a register to be read or written. The state of these inputs is ignored when the MX98902 is not in slave mode (CSX high).
PRDX	O	98	7	95	**PORT READ**: Enables data from external latch onto local bus during a memory write cycle to local memory (remote write operation). This allows asynchronous transfer of data from the system memory to local memory.

PIN DESCRIPTIONS (Continued)

A. BUS INTERFACE PINS

SYMBOL	PIN TYPE	PIN NUMBER			DESCRIPTION
		PQFP	PLCC	SQFP	
WACKX	I	96	6	93	**WRITE ACKNOWLEDGE**: Issued from system to ENC to indicate data has been written to the external latch. The ENC will begin a write cycle to place the data in local memory.
INT	O	95	5	92	**INTERRUPT**: Indicates that the MX98902 requires CPU attention after reception, transmission, or completion of DMA transfers. The interrupt is cleared by writing to the ISR. All interrupts are maskable.
RESETX	I	52	53	50	**RESET:** Reset is active low and places the MX98902 in a reset mode immediately; no packets are transmitted or received by the ENC until STA bit is set. Affects Command Register, Interrupt Mask Register, Data Configuration Register and Transmit Configuration Register. The MX98902 will execute reset within 10 BSCK cycles.
BREQ	O	45	46	42	**BUS REQUEST**: Bus Request is an active high signal used to request the bus for DMA transfers. This signal is automatically generated when the FIFO needs servicing.
BACK	I	43	45	40	**BUS ACKNOWLEDGE**: Bus Acknowledge is an active high signal that the CPU has granted the bus to MX98902. If immediate bus access is desired, BREQ should be tied to BACK. Tying BACK to VCC will result in a deadlock.
PRQ, ADS1	O, Z	42	44	39	**PORT REQUEST/ADDRESS STROBE 1**: 32-bit mode: If LAS is set in the Data Configuration Register, this line is programmed as ADS1; it is used to strobe addresses A16-A31 into external latches. (A16-A31 are the fixed addresses stored in RSAR0, RSAR1.) ADS1 will remain at TRI-STATE until BACK is received. 16-bit mode: If LAS is not set in the Data Configuration Register, this line is programmed as PRQ and is used for Remote DMA Transfers. In this mode PRQ will be a standard logic output. Note: This line will power up as TRI-STATE until the Data Configuration Register is programmed.
READY	I	41	43	37	**READY**: This pin is set high to insert wait states until a DMA transfer. The MX98902 will sample this signal at T3 during DMA transfers.
PWRX	O	39	42	36	**PORT WRITE**: Strobe used to latch data from the MX98902 into external latch for transfer to host memory during remote read transfers. The rising edge of PWRX coincides with the presence of valid data on the local bus.
RACKX	I	37	41	35	**READ ACKNOWLEDGE**: Indicates that the system DMA or host CPU has read the data placed in the external latch by the MX98902. The MX98902 will begin a read cycle to update the latch MX98902.

PIN DESCRIPTIONS (Continued)

B. NETWORK INTERFACE PINS

SYMBOL	PIN TYPE	PIN NUMBER PQFP	PLCC	SQFP	DESCRIPTION
POL	O	47	48	45	**POLARITY**: A TTL/MOS active high output. This signal is normally low. When the TPI module detects seven consecutive link pulses or three consecutive received packets with reversed polarity POLED is asserted.
TXE/TX	O	49	50	47	**TRANSMIT ENABLE/TRANSMIT**: A TTL/MOS active high output. It is asserted for approximately 50 ms whenever the MX98902 transmits data in either the AUI or TPI modes.
TEST	I	51	52	49	**FACTORY TEST INPUT**: Used to check the chip's internal function. This should be tied low during normal operation.
TXODM, TXOP TXOM, TXODP	O	55,56 58,59	54,55 56,57	56,57	**TWISTED-PAIR TRANSMIT OUTPUTS**: These high drive CMOS-level outputs are resistively combined external to the chip to produce a differential output signal with equalization to compensate for inter-symbol interference (ISI) on the twisted-pair medium.
RXIP, RXIM	I	64,65	61,62	61,62	**TWISTED-PAIR RECEIVE INPUTS**: These inputs feed a differential amplifier which passes valid data to the ENDEC module.
GDLNK	I/O	69	67	65	**GOOD LINK**: This pin has a dual input and output functions. The function is latched by the MX98902 on the rising edge of the Reset signal i.e.: on the chip returning to normal operation after reset. As an output, this pin is configured as an open drain N-channel device and is suitable for driving an LED. It will be latched as output on removal of chip reset if connected to an LED or left open circuit. Under normal conditions (the twisted-pair link is not broken) the output will be low, and the LED will be lit. The open drain output will be switched off if the twisted-pair link has been detected to be broken. It is recommended that the color of the LED be green. This output will be pulled high in AUI mode by an internal resistor of approximately 15KΩ. When this pin, which has an internal pull-up resistor to VDD, is tied low, it becomes an input and the link integrity checking is disabled.
P20M	O	70	68	66	**20 MHz**: This is a TTL/MOS-level signal. It is a buffered version of the oscillator X2. It is suitable to drive external logic, if a crystal is applied to X1 and X2.
X1	I	71	69	67	**EXTERNAL OSCILLATOR INPUT.**
X2	I	72	70	69	**X2**: This pin should normally be connected to ground. It is possible to use a crystal oscillator using X1 and X2 if certain precautions are taken.
SQUEL	I	73	-	71	**TPI SQUELCH SELECT**: This pin selects the TPI module input squelch thresholds. When tied low, the input squelch threshold on the RXIP, RXIM input complies to 10BASE-T specification. When set high, the RXIP and RXIM input operates with reduced squelch levels, allowing its use with longer lengths of cable or cable with higher losses. Internal pull down.

PIN DESCRIPTIONS (Continued)

B. NETWORK INTERFACE PINS

SYMBOL	PIN TYPE	PIN NUMBER			DESCRIPTION
		PQFP	PLCC	SQFP	
SEL	I	74	71	–	**MODE SELECT**: When high, TXP and TXM are the same voltage when idle. If low, TXP is positive with respect to TXM when idle, at the transformer's primary.
AUTP	I	75	72	72	**AUI/TPI SELECT**: A TTL level active high input that selects either the AUI interface or the TPI module for interface with the ENDEC module. When high, the AUI is selected. When low, the TPI is selected.
TXM, TXP	O	76,77	73,74	74,75	**AUI TRANSMIT OUTPUT**: Differential driver which sends the encoded data to the transceiver. The outputs are source followers which require 270Ω pulldown resistors.
RXM, RXP	I	82,83	78,79	80,81	**AUI RECEIVE INPUT**: Differential receive input pair from the transceiver.
CDM, CDP	I	84,85	80,81	82,83	**AUI COLLISION INPUT**: Differential collision pair input from the transceiver.
SNISEL	I	87	83	85	**FACTORY TEST INPUT**: For normal operation tied to VCC. When low, it enables the ENDEC module to be tested independently of the MX98902.
CRS/RX	O	88	84	86	**CARRIER SENSE/RECEIVE:** A TTL/MOS-level active high signal. It is asserted for approximately 50 ms whenever valid transmit or receive data is detected while in AUI mode or receive data is detected while in TPI mode.
COL	O	50	51	48	**COLLISION**: A TTL/MOS active high output. It is asserted for approximately 50ms whenever the MX98902A detects a collision in either the AVI or TPI modes.

PIN DESCRIPTIONS (Continued)

C. POWER SUPPLY PIN (DIGITAL)

SYMBOL	PIN TYPE	PIN NUMBER PQFP	PLCC	SQFP	DESCRIPTION
VCC		21,46 89	1, 27 47	18,43 87	**POSITIVE 5V SUPPLY PINS.**
GND		20,90 34,48 68	2, 26 39,49 64	17,32 46 ,64 88	**NEGATIVE (GROUND) SUPPLY PINS:** It is suggested that a decoupling capacitor be connected between VCC and GND pins.

D. POWER SUPPLY PINS (ANALOG)

SYMBOL	PIN TYPE	PIN NUMBER PQFP	PLCC	SQFP	DESCRIPTION
VCC		93	4	90	**VCO 5V SUPPLY PIN**: Care should be taken to reduce noise on this pin as it supplies power to the analog VCC to the Phase Lock Loop.
GND		92	3	89	**VCO GROUND SUPPLY PIN**: Care should be taken to reduce noise on this pin as it supplies ground to the analog VCC to the Phase Lock Loop.
VCC		63	60	60	**TPI RECEIVE 5V SUPPLY:** Power pin supplies 5V to the Twisted-pair Interface Receiver.
GND		66	63	63	**TPI RECEIVE GROUND:** Ground pin for the Twisted-pair Interface Receiver.
VCC		61	59	59	**TPI TRANSMIT 5V SUPPLY**: Power pin supplies 5V to the Twisted-pair Interface Transmitter.
GND		60	58	58	**TPI TRANSMIT GROUND**: Ground pin for the Twisted-pair Interface Transmitter.
VCC		81	77	79	**AUI RECEIVE 5V SUPPLY**: Power pin supplies 5V to the AUI Interface Receiver.
GND		86	82	84	**AUI RECEIVE GROUND**: Ground pin for the AUI Interface Receiver.
VCC		80	76	77	**AUI TRANSMIT 5V SUPPLY**: Power pin supplies 5V to AUI Interface Transmitter.
GND		79	75	76	**AUI TRANSMIT GROUND**: Ground pin for the AUI Interface Transmitter.

PIN DESCRIPTIONS (Continued)

E. NO CONNECTION

SYMBOL	PIN TYPE	PIN NUMBER			DESCRIPTION
		PQFP	PLCC	SQFP	
NC		3,9,13 16,19 24,35 38,40 44,53 54,57 62,67 78,91 94,97	24,25 65,66	1,5,8 16,19 24,33 38,41 44,51 52,53 68,70 73,78 91,94 97	

FUNCTIONAL DESCRIPTION

TWISTED-PAIR INTERFACE (TPI) MODULE

The TPI has five main logical functions:

1. The Smart Squelch, responsible for determining when valid data is present on the differential receive inputs (RXI±)

2. The Collision function checks for simultaneous transmission and reception of data on the TXO± and RXI± pins.

3. The Link Detector/Generator checks the integrity of the cable connecting the two twisted-pair MAUs.

4. The Jabber disables the transmitter if it attempts to transmit a longer than legal packet.

5. The TX Driver & Pre-emphasis transmit Manchester encoded data to the twisted-pair network via the summing resistors and transformer/filter.

SMART SQUELCH

To make sure that impulse noise on the receive inputs will not be mistaken for a valid signal, the ENC carries out an intelligent receive squelch on the RX± differential inputs. The squelch circuitry uses a mix of amplitude and timing measurements to gauge whether the data on the twisted-pair inputs is valid.

Smart squelch checks the signal at the start of packet and any pulses that do not exceed the squelch level, either positive or negative, depending on polarity, is rejected. After this first squelch level is overcome the opposite squelch level must be exceeded within 150 ns. Finally, the signal goes beyond the original squelch level within a further 150 ns in order for the input waveform not to be rejected. The procedure entails the loss of at least three bits at the start of each packet.

When these conditions are satisfied a control signal will be generated to show the remainder of the circuitry that valid data is present. Then the smart squelch circuitry is reset.

Valid data is deemed present until either squelch level has not been generated for a time longer than 150 ns, which shows End of Packet. If good data is detected, the squelch levels are reduced to contain the noise effect which may lead to premature End of Packet detection.

COLLISION

A collision is detected by the TPI module when the receive and transmit channels are active simultaneously. If the TPI is receiving when a collision is detected it is reported to the controller immediately. If, however, the TPI is transmitting when a collision is detected the collision is not reported until seven bits have been received while in the colliision state. This prevents a collision being reported incorrectly due to noise on the network. The signal to the controller remains for the duration of the collision.

Approximately 1µs after the transmission of each packet a signal called the Signal Quality Error (SQE) consisting of typically 10 cycles of 10 MHz is generated. This 10 MHz signal, also called the Heartbeat, ensures the continued functioning of the collision circuitry.

LINK DETECTOR/GENERATOR

This is a timer circuit that generates a link pulse as shown in the 10BASE-T specification. With a width of 100 ns, the pulse is transmitted every 16 ms on the TXO+ output in the absence of transmit data.

The pulse checks the integrity of the connection to the remote MAU, and the link detection circuit checks for valid pulses from the remote MAU. The link detector will disable the transmit, receive, and collision detection functions if valid link pulses are not received.

To determine that a good twisted-pair link exists, the GDLNK output directly drives an LED; the LED will be on during normal conditions.

JABBER

Whenever the transmitter is active for greater than 52 ms, the jabber timer monitors the transmitter and disables the transmission. In this case, the transmitter is then disabled for the time that ENDEC module's inter-

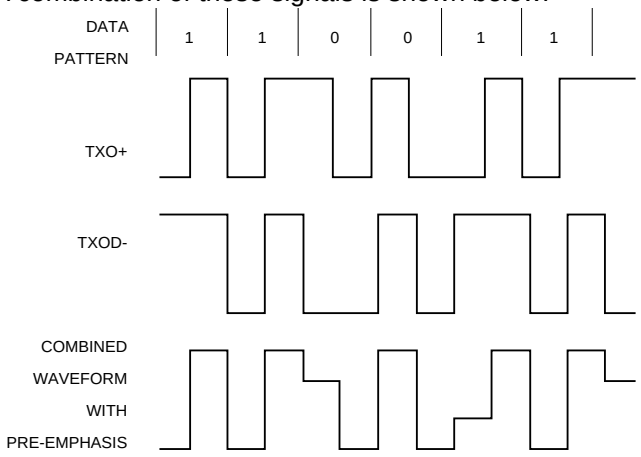
nal transmit enable is asserted. This signal has to be deasserted for about 750 ms before the Jabber re-enables the transmit outputs.

TRANSMIT DRIVER

The transmitter has four signals, the true and complement Machester-encoded data (TXO±). These signals may be delayed by 50 ns (TXOD±).

These four signals are combined, TXO+ with TXOD- and TXO- with TXOD+. Known as digital pre-emphasis, this process is required to compensate for the twisted-pair cable which acts like a low-pass filter and can greatly weaken the 10 MHz (50 ns) pulses of the Manchester-encoded waveform than the 5 MHz (100 ns) pulses.

A combination of these signals is shown below:



STATUS INFORMATION

This information is shown at the ENC on the CRS/RX, TXE/TX, COL and POL outputs as decribed in the pin description table. These outputs can drive status LEDs by means of an appropriate driver circuit.

Normally low, the POL output will be driven high when seven consecutive link pulses or three consecutive link pulses having reversed polarity are detected. A wiring error at either end of the TPI cable can cause polarity reversal. Upon detection of this reversal the condition is latched and POL is asserted. Correcting this error is the TP1 and will also decode received data correctly, thus getting rid of the need to check the wiring error.

MANCHESTER ENCODER AND DIFFERENTIAL DRIVER

On the transformer's secondary, the differential transmit pair drives up to 50 meters of twisted-pair AUI cable. These outputs are source followers requiring two 270Ω pulldown resistors to ground.

The MX98902 enables both half-step and full-step to be compatible with Ethernet and IEEE 802.3. Transmit+ is positive as regards Transmit- with the SEL pin low (for Ethernet 1). With SEL high (for IEEE 802.3), Transmit+ and Transmit- are equal when idle, thus providing zero differential voltage to operate with transformer-coupled loads.

MANCHESTER DECODER

This decoder is composed of a differential receiver and a PLL to separate a Manchester-decoded data stream into internal clocks signals and data. When using the standard 78Ω transceiver drop cable, see that the differential input must be externally terminated with two 39Ω resistors connected in series. These resistors are optional in Thin Ethernet applications. A squelch circuit at the input rejects signals with levels less than -175 mV to prevent noise from triggering the decoder. And signals negative than -300 mV are decoded; data becomes valid within 5 bit times. The MX98902 may be able to take bit jitter up to 18 ns in the data that is received.

COLLISION TRANSLATOR

If the Ethernet transceiver, when in AUI mode, detects a collision, it generates a 10 MHz signal to the differential collision inputs (CD±) of the MX98902. When these inputs are active, the MX98902 uses this signal to cancel its current transmission and reschedule another one.

The collision differential inputs are ended in the same way as the differential receive inputs. The squelch circuitry is also similar, rejecting pulses with levels less than -175 mV.

FUNCTIONAL DESCRIPTION (Continued)

RECEIVE DESERIALIZER

The receive deserializer starts to work when the input signal Carrier Sense is asserted. It allows incoming bits to be shifted into the shift register by the receive clock provided by the SNC (Serial Network Converter). The serial receive data is also routed to the CRC generator/ checker to detect CRC code. The receive deserializer includes a synch detector that detects the SFD (Start of Frame Delimiter) to establish where byte boundaries within the serial bit stream are located, i.e., when a 1,1 bit sequence is detected, it begins to collect data. After every eight receive clocks, the byte-wide data is transferred to the 16-byte FIFO (two 8-byte FIFOs) alternatively and the receive byte count is incremented. The first six bytes after the SFD are checked for valid comparison by the Address Recognition Logic. If the address recognition Logic does not recognize the packet, the FIFO is cleared.

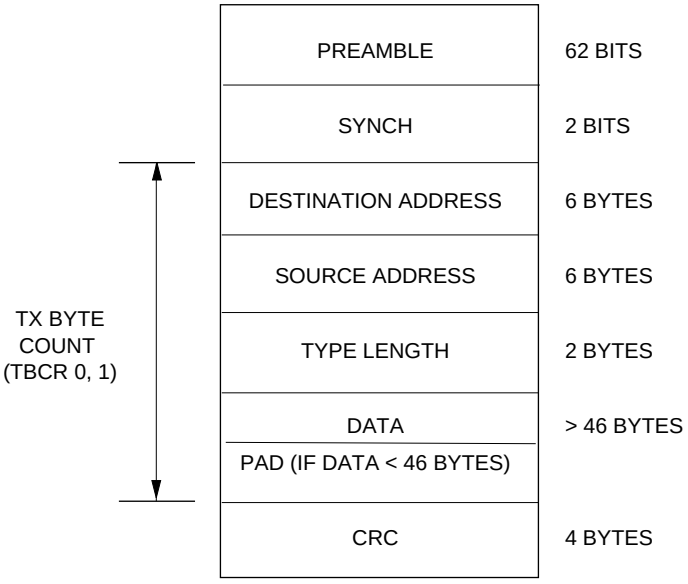
ADDRESS RECOGNITION LOGIC

The address recognition logic compares the destination address field (first 6 bytes of the received packet) with the physical address registers stored in the address register array, one byte at a time, by the 8th receive clock. If any one of the six bytes does not match the preprogrammed physical address, the protocol PLA rejects the packet. This means that the packet does not belong to the node. All multicast destination addresses are filtered using a hashing technique by latching the 6 most significant bits of the CRC generator. If the multicast address indexes a bit that has been set in the filter bit array of the multicast address register array, the packet is accepted. Otherwise, it is rejected by the Protocol PLA. Each destination address is also checked for all 1's which is the reserved broadcast address.

PACKET TRANSMISSION

A complete transmit packet consists of Preamble, Synch, Data, and CRC fields. The data field is a contiguous assembled packet of Destination Address. Source Address, Length Field, and Data with the format shown below. During transmit, Page Start Address Register (TPSR) and the Transmit Byte Count Registers (TBCR0,1), control the DMA transfer. As a transmit command is issued to ENC, the packet of data in buffer memory pointed 0 by these registers will be moved into the FIFO. The ENC will generate and append the preamble, synch and CRC fields. In addition, if transmitting data is smaller than 46 bytes, the packet must be padded to a minimum size of 64 bytes. The programmer is responsible for adding and stripping pad bytes.

GENERAL TRANSMIT PACKET FORMAT



CONDITIONS REQUIRED TO BEGIN TRANSMISSION

To initiate transmission of a packet, the TPSR (Transmit Page Start Register) and TBCR0, TBCR1 (Transmit Byte Count Registers) must be initialized and the TXP bit in the Command Register must be set. The ENC will start to prefetch transmit data from memory, if no neception is currently receiving. Three conditions must be met before transmission:

1. The Interframe Gap Timer has timed out the first 6.4μs of the Interframe Gap.

2. At least one byte has entered the FIFO, which means that burst transfer has begun.

3. If collision occurs in the ENC, the backoff timer must expire before retransmit.

FUNCTIONAL DESCRIPTION (Continued)

If carrier sense is asserted before a byte has been loaded into the FIFO, the ENC will become a receiver.

COLLISION RECOVERY

If transmission has collided with another station, the buffer management logic, which monitors the transmit circuitry will reset the FIFO and restore the Transmit DMA pointers for retransmission of the packet. When collision is detected, the COL bit in TSR will be set and the NCR (Number of Collisions Register) will be incremented. If each of the 15 retransmissions results in a collision, the transmission will be terminated and the ABT bit in the TSR will be set. If excessive collisions (i.e., 16 consecutive collisions) are encountered, NCR reads as zeros and transmission is aborted.

TRANSMIT PACKET ASSEMBLY FORMAT

The following diagrams show the format for assembling packets before they are transmitted for different byte-ordering schemes. The various formats are selected in the Data Configuration Register.

DA = Destination Address
SA = Source Address
T/L = Type/Length Field

BIT D15 D8 D7 D0

DA1	DA0
DA3	DA2
DA5	DA4
SA1	SA0
SA3	SA2
SA5	SA6
T/T1	T/L0
DATA1	DATA0

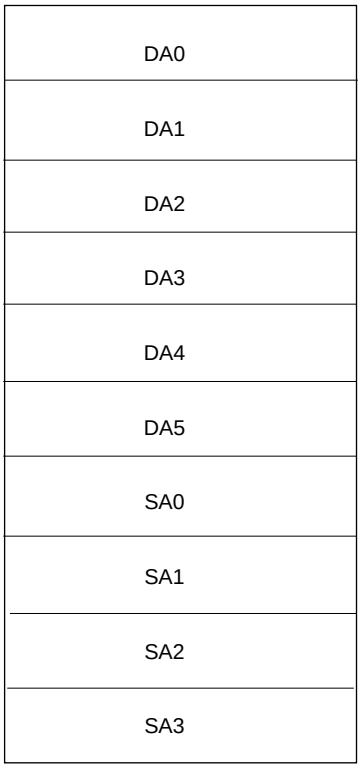
BOS = 0, WTS - 1 in Data Configuration Register.
This format is used with Series 32000, 808X-type processors.

BIT D15 D8 D7 D0

DA0	DA1
DA2	DA3
DA4	DA5
SA0	SA1
SA2	SA3
SA4	SA5
T/L0	T/L1
DATA0	DATA1

BOS = 1, WTS = 1 in Data Configuration Register.
This format is used with 68000-type processors.

FUNCTIONAL DESCRIPTION (Continued)



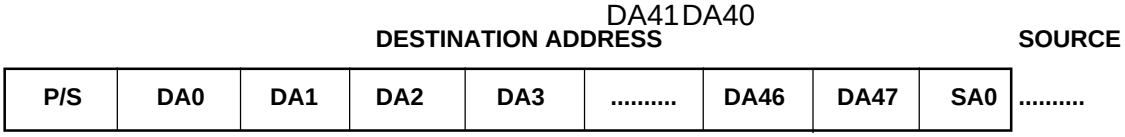
BOS = 0, WTS= 1 in Data Configuration Register.
This format is used with general 8-bit CPUs.

FUNCTIONAL DESCRIPTION (Continued)

PHYSICAL ADDRESS REGISTERS (PAR0-PAR5)

The physical address registers are used to compare the destination address of incoming packets for rejecting or accepting packets. It compares physical addresses in PAR0-PAR5 with incoming data one byte at a time. The bit assignment shown below relates the sequence in PAR0-PAR5 to the bit sequence of the received packet.

	D7	D6	D5	D4	D3	D2	D1	D0
PAR0	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
PAR1	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
PAR2	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
PAR3	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
PAR4	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
PAR5	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40



NOTE: P/S = Preamble, Synch
DA0 = Physical/Multicast Bit

FUNCTIONAL DESCRIPTION (Continued)

DIRECT MEMORY ACCESS CONTROL (DMA)

The DMA capabilities of the ENC greatly simplify use of the MX9890 in typical configuration. The local DMA channel transfers data between FIFO, which is inside the ENC, and memory which is outside the ENC. There are two kinds of local DMA type: Local DMA Read and Local DMA Write. Local DMA Read moves data from memory into FIFO on transmission. Should a collision occur (up to 15 times), the packet is retransmitted with no processor intervention. Local DMA Write transfers data from FIFO to memory on reception.

A remote DMA channel is also provided on the ENC to accomplish transfers between a buffer memory and a system memory whenever the I/O map board design is required. The two DMA channels (local DMA and remote DMA) can alternatively be combined to form a single 32-bit address with 8- or 16-bit data.

DUAL DMA CONFIGURATION

Network activity is isolated on a local bus, where the ENC's local DMA channel performs burst transfers between the buffer ring and the ENC's FIFO. The remote DMA transfers data between the buffer ring and the host memory by means of a bidirectional I/O port. Meanwhile, remote DMA provides local addressing capability and is used as a slave DMA by the host. Host side addressing must be provided by a host DMA or the CPU. The ENC allows Local and Remote DMA operations to be interleaved because the ENC takes care of the bus arbitration problem itself.

SINGLE CHANNEL DMA OPERATION

If desirable, the two DMA channels can be combined to provide a 32-bit DMA address. The upper 16 bits of the 32-bit address provided by the remote DMA channel are static and are used to point to a 64-kbyte (or 32k word) page of memory where packets are to be received or transmitted. The lower 16 bits of the 32-bit address provided by Local DMA channel are dynamic and are used to point to a 64-kbyte (or 32 kword) offset of memory.

LOOPBACK MODE

Mode1:LoopbackThroughTheNEC Module(LB1=0,LBO=1)
If this loopback is used, the ENC Module's serializer is connected to the deserializer.

Mode 2 : Loopback through the MCC Module (LB1=1, LBO=0)
If this loopback is to be performed through the MCC, the MX98902 provides a control (LBK) that forces the MCC module to loopback all signals.

Mode3 : Loopback to cable (LB1=1, LBO=1)
Packets can be transmitted to the cable in loopback mode to check all of the transmit and receive paths and cable itself

Note : Collision and Carrrier Sense can be generated by the MCC module and are Masket by the ENC module. It is not possible to go directly between the loopback modes, it is necessary to return to normal (OOH) when changing modes.

READING THE LOOPBACK PACKET

The last 8 bytes of a received packet can be examined by 8 consecutive reads of the FIFO register. The FIFO pointer is incremented after the rising edge of the CPU's read strobe by internally synchronizing and advancing the pointer. This may take up to four bus clock cycles, if the pointer has not been incremented by the time the CPU reads the FIFO registers again, the MX98902 will insery wait states..

ALIGNMENT OF THE RECEIVED PACKET IN THE FIFO

Reception of the packet in the FIFO begins at location zero, after the FIFO pointer reaches the last location in the FIFO, the pointer wraps to the top of the FIFO overwriting the previously received data. This process is continued until the last byte is received. The MX98902 then appends the received byte count in the next two locatioms of the FIFO. The contents of the Upper Byte Count are also copied to the next FIFO location. The number of bytes used in the loopback packet determines the alignment of the FIFO. The alignment for a 8 X N byte packet is shown below.

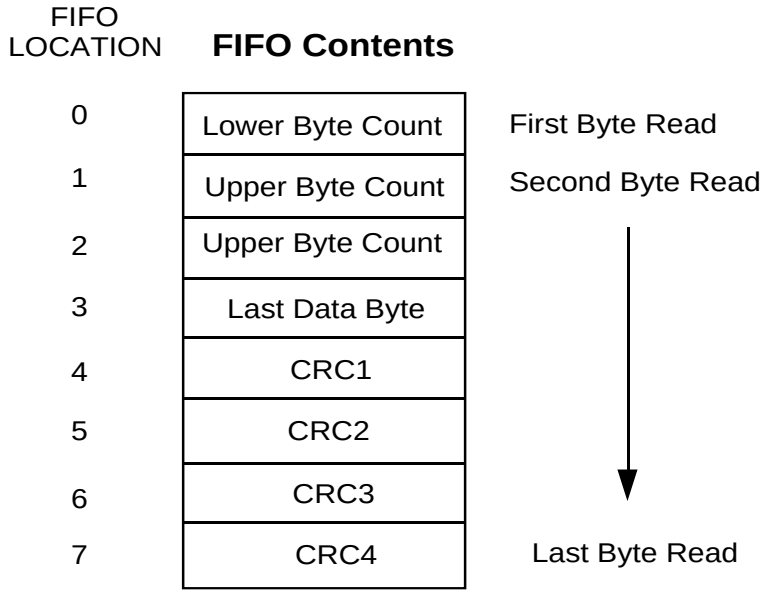


Figure 5.7.3 FIFO Alignment for 8 X N byte

RESTRICTIONS DURING LOOPBACK

The FIFO is split into two halves, one half is used for transmission and the other for reception. Only 8 bit fields can be fetched from memory so two tests are requires (shown in figure 5.7.4) for 16-bit system to verify integrity of the entire data path. During loopback the maximum latency from the assertion of BREQ to BACK is 2.Ous. Figure A in figure 5.7.4 verify the data path for 680x0 CPU yet figure B verify the data path for 32000/80x86 CPUs.

LS Byte(AD8-15) MS Byte(AD0-7)

	Destination
	Sourec
	Length
	Data
	CRC

WTS="1" BOS="1" (DCR bits)

Figure A. 680X0 CPU data path verification during loopback

LS Byte(AD8-15) MS Byte(AD0-7)

Destination	
Sourec	
Length	
Data	
CRC	

WTS="1" BOS="1" (DCR bits)

Figure B. 32000/80x86 CPU data path verification during loopback

Figure 5.7.4 Data path verification during

EXAMPLES

The following examples show what results can be expected from a properly operating MX98902 during loopback. The restrictions and results of each type of loopback are listed for reference. The loopback tests are divided into two sets of test. One to verify the data path, CRC generation and byte count through all three paths. the second set of test uses internal loopback to verify the receiver's CRC checking and address recognition. For all of the tests the DCR was programmed to 40H.

Path	TCR	RCR	TSR	RSR	ISR
MX9890 Internal	02	1F	53 (Note 1)	02 (Note 2)	02 (Note 3)

Note 1 : Since carrier sense and collision detect are generated in the MCC module, they are blocked during ENC loopbak. Carrier and CD hertbeat are not seen and the CRS and CDH bits are set.
Note 2 : CRC errors are always indicated by the receiver if CRC is appended by the transmitter.
Note 3 : Only the PTX bit in the ISR is set, the PRX bit is only set if status is written to memory. In loopback this action does not occur and the PRX bit remains 0 for all loopbak modes.
Note 4 : All values are hex.

Path	TCR	RCR	TSR	RSR	ISR
Loopback to MCC	04	1F	43 (Note 1)	02	02

Note 1 : CDH is set, CRS is not set since it is generated by the external MCC module.

Path	TCR	RCR	TSR	RSR	ISR
Loopback to TPI	06	1F	03 (Note 1)	02	02 (Note 2)

Note 1 : CDH should not be set. The TSR however , could also contain 01H,03H,07H and a variety of other Values depending on whether collisions were encountered or the packet was deferred. If collision was encountered during sending preamble, then CRS of TSR may be set depending on whether Receive clock is synchrounous to transmit clock or not.
Note 2 : The ISR will contain 08H if packet is not transmittable.
Note 3 : During exteral loopback the MX98902 is now exposed to network traffic. It is threrfore possible for the contents of both the Receive portion of the FIFO and the RSR to be corrupted by any other packer on the network. Thus in a live network the contents of the FIFO and RSR should not be depended on. The MX98902 will still abide by the standard CSMA/CD protocol in external loopbak mode. (i.e., The network will not be disturbed by the loopback packet.)
Note 4 : All values are hex.

CRC and Address Recognition

The next three tests exercise the address recognitioon logic and CRC. There tests should be performed using internal loopback only so that the MX98902 is isolated from interference from the network. These tets also require the capability to generaye CRC in software (i.e., CRC inhibibit by transmitter).

The address recognition logic cannot be directly tested. The CRC and FAE bits in the RSR are only set if the address in the packet matches the address filter (PARO - PAR5). If errors are expected to be set and tyey are not set, the packet has been rejected on the basis of an address mismatch. The following sequence of packets will test the address recognition logic. The DCR should be set to 40H and the TCR should be set to 03H with a software generated CRC.

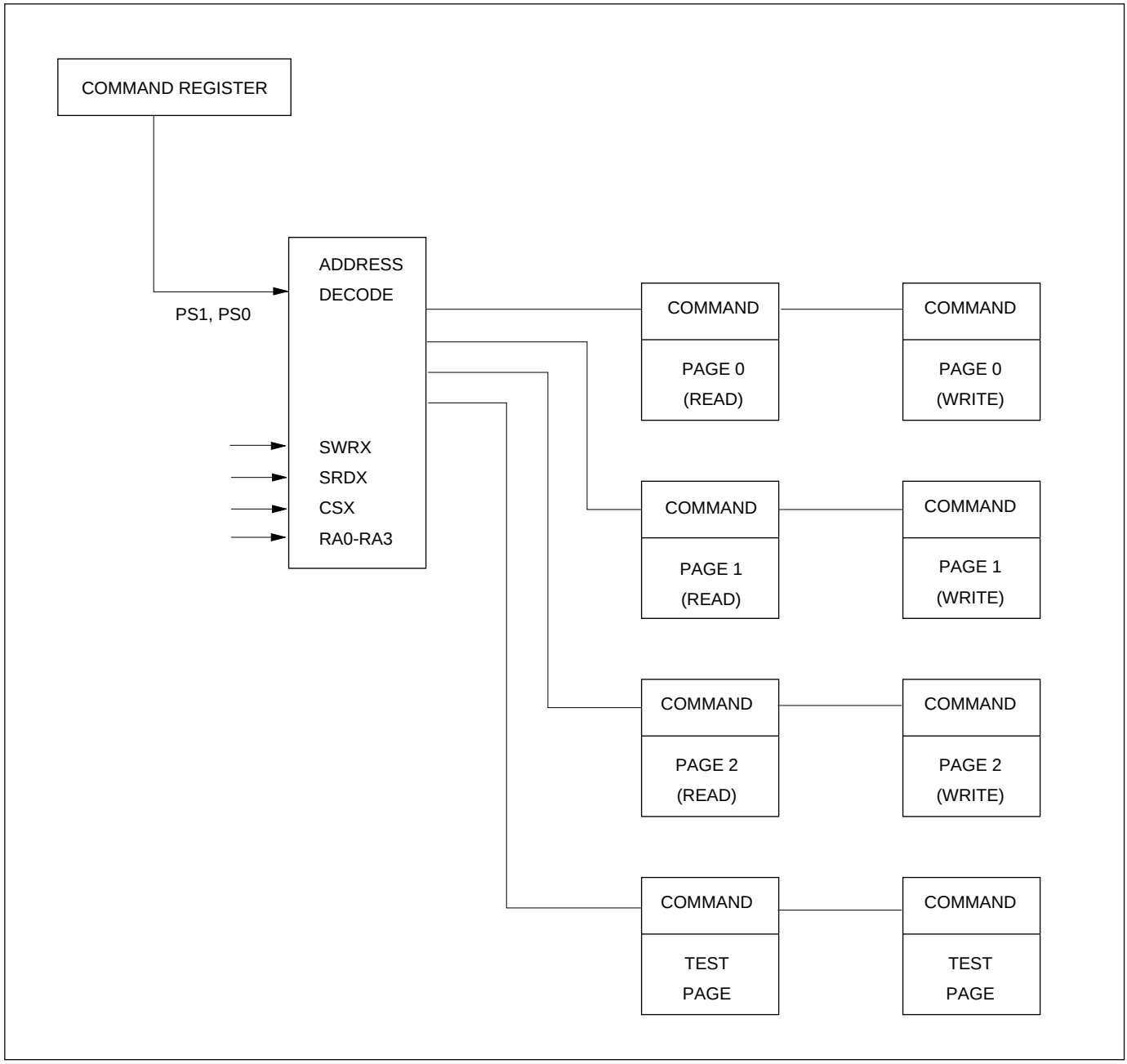
Packet Conyents			Results
Test	**Address**	**CRC**	**RSR**
Test A	Matching	Good	01 (Note 1)
Test B	Matching	Bad	02 (Note 2)
Test C	Non-Matching	Bad	01

Note 1 : Status will read 21H if multicast address used
Note 2 : Status will read 22H if multicast address used
Note 3 : In test A, the RSR is set up. In test B the address is found to match since the CRC is flagged as bad. Test C proves that the address recognition logic can distinguish a bad address and does not notify the RSR of the bad CRC. The receiving CRC is proven to work in test A and test B.
Note 4 : All values are hex.

INTERNAL REGISTERS

All internal registers are mapped into three pages and selected by two bits, PS1 and PS0, of Command Register. Input pins RA0-RA3 are used to address these internal registers which are 8-bit wide and are commonly accessed during ENC register read/write operation. For user's convenience, registers that are commonly accessed during ENC operation are mapped into page 0. Page 1 registers are used primarily for initialization while Page 2 registers are used for diagnostic. Partitioned registers make one write/read cycle possible for accessing those commonly used registers.

REGISTER ADDRESS MAPPING



REGISTER DESCRIPTION

A. Command Register (CR) 00H (Read/Write)

The Command Register is used to take the controller on/off line (STA and STP bits), initiate transmissions (TXP bit), enable or disable Remote DMA operations (RD2, RD1 and RD0 bits), and select register pages (PS1 and PS0). To issue a command, the microprocessor sets the corresponding bit(s). In addition, commands may be overlapped following the guidelines below:

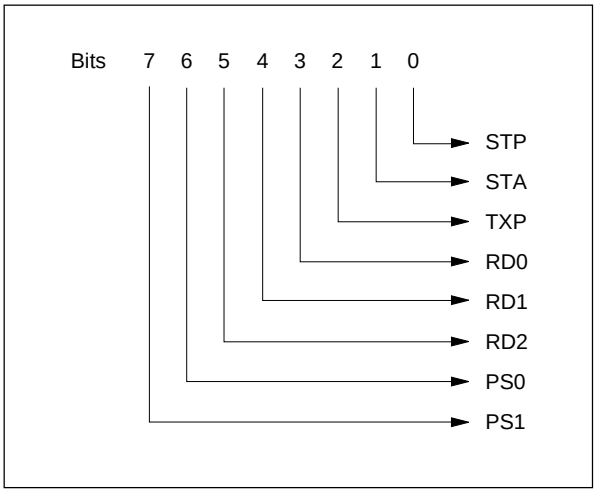
1. If a remote DMA operation overlaps a transmission, RD0, RD1 and RD2 must be written with the desired values, and a "0" or "1" may be written to the TXP bit because writing a "0" to TXP has no effect after transmission is activated.

2. A remote write DMA may not overlap remote read operation and vice versa. Each operation must either be completed or aborted before starting the other one.

3. If a transmit command overlaps with a remote DMA operation, bits RD2, RD1 and RD0 must be maintained for the remote DMA command when setting the TXP bit.

NOTE: If a remote DMA command is reissued while giving the transmit command, the DMA will complete the process immediately if the remote byte count registers (RBCR1 and RBCR0) have not been reinitialized, i.e., one has to program RBCR0 and/or RBCR1 every time when one needs remote DMA service.

4. Bits PS1, PS0, RD2 and STP can be set at any moment.



REGISTER DESCRIPTION (Continued)

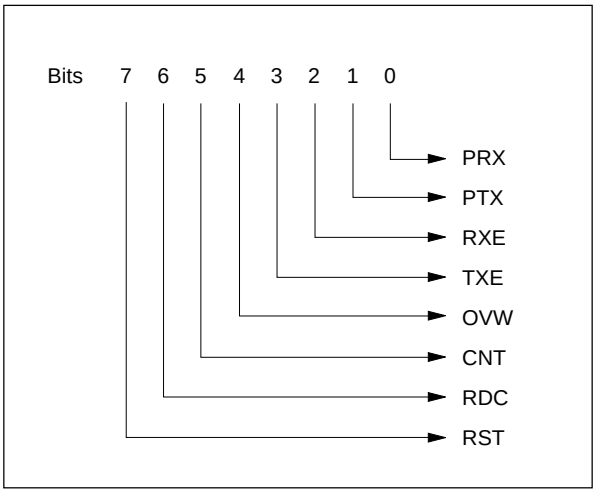
A. COMMAND REGISTERS (Continued)

SYMBOL	BIT	DESCRIPTION
STP	D0	**STOP**: Software reset command, takes the controller offline; no Packets will be received or transmitted if this bit is set high. Any reception or transmission in progress will enter the reset state after operation is completed. This bit must be cleared and the STA bit must be set high to exit the reset state. The software reset is executed only when the RST bit in the ISR is set to 1. STP powers up high. Note: If the ENC has previously been in start mode and the STP is set, both the STP and STA bits will remain set.
STA	D1	**START**: This bit is used to activate the ENC after either power-up, or when the ENC has been placed in a reset mode by software command or error. STA powers up low.
TXP	D2	TRANSMIT PACKET: This bit must be set to initiate transmission of a packet only after the Transmit Byte Count (TBCR1 and TBCR0) and Transmit Page Start register (TPSR) have been programmed. TXP is internally reset either after the transmission is completed or aborted.
PD0, PD1, PD2	D3, D4, D5	**REMOTE DMA COMMAND**: These three encoded bits control operation of the Remote DMA channel. RD2 can be set to abort any Remote DMA command in progress. The Remote Byte Count Registers should be cleared by host whenever a Remote DMA has been aborted. The Remote Start Addresses are not restored to the starting address if the Remote DMA is aborted. Hence, for another remote DMA operaton, host should provide a starting address for ENC in order to operate correctly. **RD2 RD1 RD0** 0 0 0 Not Allowed 0 0 1 Remote Read 0 1 0 Remote Write 0 1 1 Send Packet 1 X X Abort/Complete Remote DMA (Note) Note: If a remote DMA operation is aborted and the remote byte count has not decremented to zero, PRQ will remain high. A read acknowledge (RACKX) or a write acknowledge (WACKX) will reset PRQ low.
PS0, PS1	D6, D7	**PAGE SELECT**: These two encoded bits select which register page is to be accessed with addresses RA0-3 **PS1 PS0** 0 0 Register Page 0 0 1 Register Page 1 1 0 Register Page 2 1 1 Reserved

REGISTER DESCRIPTION (Continued)

B. INTERRUPT STATUS REGISTER (ISR) 07H (READ/WRITE)

This register is accessed by the host processor to determine the cause of an interrupt. Any interrupt can be masked in the Interrupt Mask Register (IMR). Individual interrupt bits are cleared by writing a "1" into the corresponding bit of the ISR. The INT signal is active as long as any unmasked signal is set; it will not go low until all unmasked bits in this register have been cleared. The ISR must be cleared after power-up by writing it with all 1's.



SYMBOL	BIT	DESCRIPTION
PRX	D0	**PACKET RECEIVED**: Indicates packet received with no errors.
PTX	D1	**PACKET TRANSMITTED**: Indicates packet transmitted with no errors.
RXE	D2	**RECEIVE ERROR**: Indicates that a packet was received with one or more of the following errors: - CRC Error - Frame Alignment Error - FIFO Overrun - Missed Packet
TXE	D3	**TRANSMIT ERROR**: Set when packet is transmitted with one or more of the following errors: - Excessive Collisions - FIFO Underrun
OVW	D4	**OVERWRITE WARNING:** Set when receive buffer ring storage resources have been exhausted. (Current Pointer has reached Boundary Pointer)

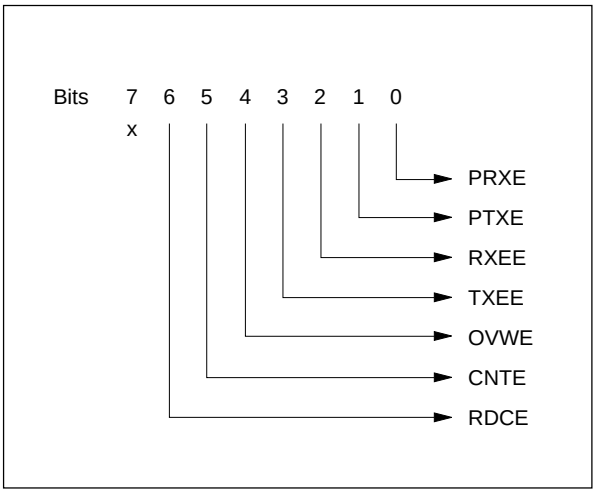
REGISTER DESCRIPTION (Continued)

B. INTERRUPT STATUS REGISTER (ISR) 07H (READ/WRITE) (Contiuned)

SYMBOL	BIT	DESCRIPTION
CNT	D5	**COUNTER OVERFLOW**: Set when MSB of one or more of the Network Tally Counters has been set.
RDC	D6	**REMOTE DMA COMPLETE**: Set when Remote DMA operation has been completed.
RST	D7	**RESET STATUS**: Set when ENC enters reset state and cleared when a start command is issued to the CR. This bit is also set when a Receive Buffer Ring overflow occurs and is cleared when one or more packets has been removed from the ring. Writing to this bit has no effect. Note: This bit does not generate any interrupt; it is merely a status indicator.

C. INTERRUPT MASK REGISTER (IMR) 0FH (WRITE)

The Interrupt Mask Register is used to mask interrupts. Each interrupt mask bit corresponds to a bit in the Interrupt Status Register (ISR). If an interrupt mask bit is set, an interrupt will be issued whenever the corresponding bit in the ISR is set. If any bit in the IMR is set low, an interrupt will not occur when the bit in the ISR is set. The IMR powers up all zeros.



REGISTER DESCRIPTION (Continued)

C. INTERRUPT MASK REGISTER (IMR) 0FH (WRITE) (Continued)

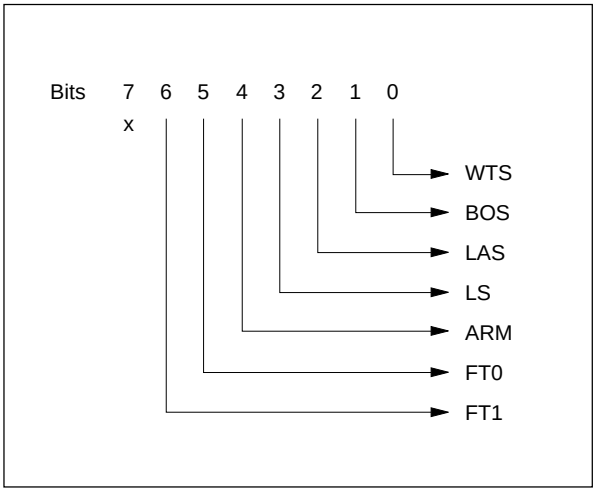
SYMBOL	BIT	DESCRIPTION
PRXE	D0	**PACKET RECEIVED INTERRUPT ENABLE** 0: Disables Interrupt when packet is received. 1: Enables Interrupt when packet is received.
PTXE	D1	**PACKET TRANSMITTED INTERRUPT ENABLE** 0: Disables Interrupt when packet is transmitted. 1: Enables Interrupt when packet is transmitted.
RXEE	D2	**RECEIVE ERROR INTERRUPT ENABLE** 0: Disables Interrupt when packet is received with error. 1: Enables Interrupt when packet is received with error.
TXEE	D3	**TRANSMIT ERROR INTERRUPT ENABLE** 0: Disables Interrupt when packet transmission results in error. 1: Enables Interrupt when packet transmission results in error.
OVWE	D4	**OVERWRITE WARNING INTERRUPT ENABLE** 0: Disables Interrupt when Buffer Management Logic lacks sufficient buffers to store an incoming packet. 1: Enables Interrupt when Buffer Management Logic lacks sufficient buffers to store an incoming packet.
CNTE	D5	**COUNTER OVERFLOW INTERRUPT ENABLE** 0: Disables Interrupt when MSB of one or more of the Network Statistics Counters has been set. 1: Enables Interrupt when MSB of one or more of the Network Statistics Counters has been set.
RDCE	D6	**DMA COMPLETE INTERRUPT ENABLE** 0: Disables Interrupt when Remote DMA transfer has been completed. 1: Enables Interrupt when Remote DMA transfer has been completed.
RESERVED	D7	**Reserved**

REGISTER DESCRIPTION (Continued)

D. DATA CONFIGURATION REGISTER (DCR) 0EH (WRITE)

C. INTERRUPT MASK REGISTER (IMR) 0FH (WRITE) (Continued)

This register is used to program the ENC for 8- or 16-bit memory interface, select normal or loopback operation, select byte ordering in 16-bit application, and establish FIFO threshold. The DCR must be initialized prior to loading the Remote Byte Count Registers. LAS is set on power-up.



SYMBOL	BIT	DESCRIPTION
WTS	D0	**WORD TRANSFER SELECT** 0: Selects byte-wide DMA transfers 1: Selects word-wide DMA transfers WTS establishes byte or word transfer for both Remote and Local DMA transfers. Note: When word-wide mode is selected, up to 32K words are addressable; A0 remains low.
BOS	D1	**BYTE ORDER SELECT** 0: MS byte placed on AD15-AD8 and LS byte on AD7-AD0 (32000, 80x86) 1: MS byte placed on AD7-AD0 and LS byte on AD15-AD8 (68x0); ignored when WTS is low.
LAS	D2	**LONG ADDRESS SELECT** 0: Dual 16-bit DMA mode 1: Single 32-bit DMA mode When LAS is high, the contents of the Remote DMA Registers RSAR0, 1 are issued as A16-A31. Power up high.

REGISTE DESCRIPTION (Continued)

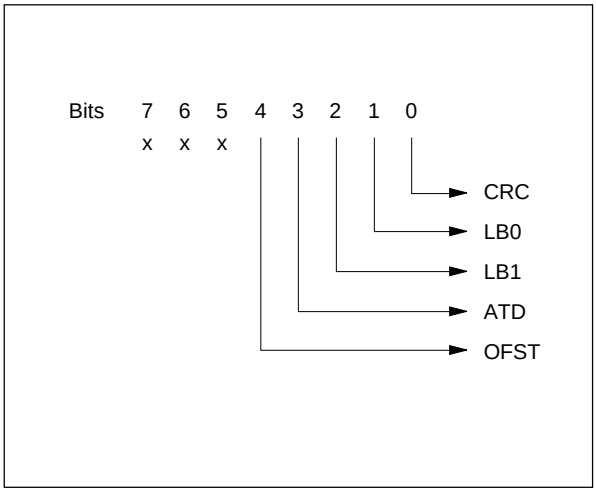
D. DATA CONFIGURATION REGISTER (DCR) 0EH (WRITE) (Continued)

SYMBOL	BIT	DESCRIPTION
LS	D3	**LOOPBACK SELECT** 0: Loopback mode select. Bits LB0, LB1 o f the TCR must be programmed for loopback operation. 1: Normal Operation. Ignore the values of LB1 and LB0 of TCR.
ARM	D4	**AUTO-INITIALIZE REMOTE** 0: Send Command not excuted, all packets removed from Buffer Ring under program control. 1: Send Command excited, Remote DMA auto-initilized to remove packets from Buffer Ring Note: Send Command cannot be used with 68x0-type processors and should be issued right after reception of packet is completed.
FT0, FT1	D5,D6	**FIFO THRESHOLD SELECT**: Encoded FIFO threshold; establishes point at which bus is requested when filling or emptying the FIFO. During reception, the FIFO threshold indicates the number of bytes (or words) the FIFO has filled serially from the network before bus request (BREQ) is asserted. During transmission, the FIFO threshold indicates the number of bytes (or words) the FIFO has filled from the Local DMA before BREQ is asserted. Thus, the transmission threshold is 16 bytes less the received threshold. Note: FIFO threshold setting determines the Local DMA burst length. RECEIVE THRESHOLDS **FT1 FT0 WORD WIDE BYTE WIDE** 0 0 1 word 2 bytes 0 1 2 words 4 bytes 1 0 4 words 8 bytes 1 1 6 words 12 bytes

REGISTER DESCRIPTION (Continued)

E. TRANSMIT CONFIGURATION REGISTER (TCR) 0DH (WRITE)

Before transmission of a packet on the network, the Transmit Configuration Register is configured to establish the actions of the transmitter section of the ENC during transmission of a packet on the network. LB1 and LB0 select loopback mode power-up as 0.



SYMBOL	BIT	DESCRIPTION
CRC	D0	**INHIBIT CRC** 0: CRC appended by transmitter 1: CRC inhibited by transmitter In loopback mode CRC can be enabled or disabled to test the CRC logic.
LB0, LB1	D1, D2	**ENCODED LOOPBACK CONTROL**: The type of loopback to be performed is determined by these encoded bits. **LB1** **LB2** Mode 0 0 0 Normal Operation Mode 1 0 1 Internal Loopback Mode 2 1 0 External Loopback to ENDEC Mode 3 1 1 External Loopback to TPI
ATD	D3	**AUTO TRANSMIT DISABLE**: Setting this bit allows another station to disable the ENC's transmitter by transmission of a particular multicast packet. The transmitter can be re-enabled by resetting this bit or by reception of a second particular multicast packet. 0: Normal Operation 1: Reception of multicast address hashing to bit 62 disables transmitter; reception of multicast address hashing to bit 63 enables transmitter.

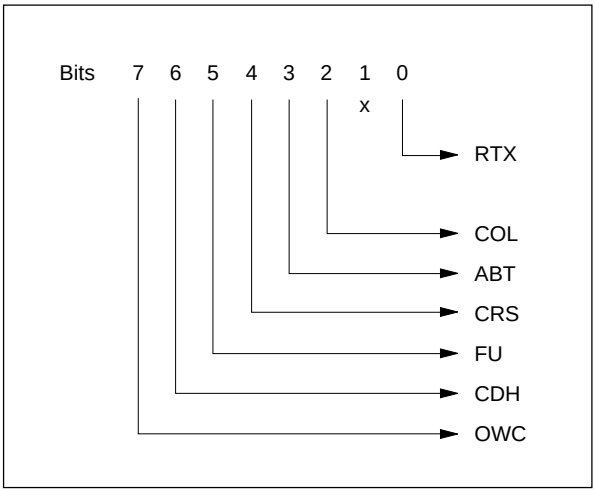
REGISTER DESCRIPTION (Continued)

E. TRANSMIT CONFIGURATION REGISTER (TCR) 0DH (WRITE) (Continued)

SYMBOL	BIT	DESCRIPTION
OFST	D4	**COLLISION OFFSET ENABLE**: This bit modifies the backoff algorithm to allow prioritization of modes. 0: Normal Backoff algorithm 1: Forces Backoff algorithm modification to 0 to 2 min (3+n, 10) slot times for first three collisions, then follows standard backoff.(For first three collisions station has higher average backoff delay making a low priority mode.)
RESERVED	D5	**Reserved**
RESERVED	D6	**Reserved**
RESERVED	D7	**Reserved**

F. TRANSMIT STATUS REGISTER (TSR) 04H (READ)

Each particular bit of this register is set when the corresponding event occurs on the media during transmission of a packet. The contents of this register are not specified until after the first transmission and are cleared upon the start of next transmission initiated by the host. A read of this register is necessary after each transmission.



REGISTER DESCRIPTION (Continued)

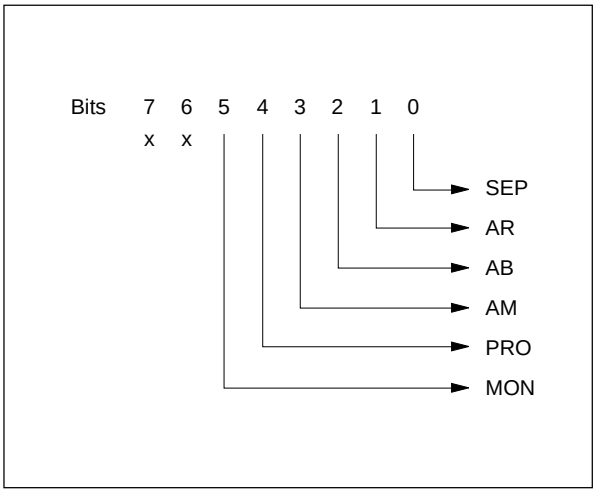
F. TRANSMIT STATUS REGISTER (TSR) 04H (READ) (Continued)

SYMBOL	BIT	DESCRIPTION
PTX	D0	**PACKET TRANSMITTED**: Set when transmitted without error. (No excessive collisions or FIFO underrun) (ABT= "0", FU = "0")
	D1	**Reserved**
COL	D2	**TRANSMIT COLLIDED:** Set when transmission collided at least once with another station on the network. The number of collisions is recorded in the Number of Collisions Registers (NCR).
ABT	D3	**TRANSMIT ABORTED**: Set when transmission is aborted because of excessive collisions. (Total number of transmission attempts equals 16).
CRS	D4	**CARRIER SENSE LOST**: Set when carrier is lost during transmission of a packet. Carrier Sense is monitored from the end of Preamble/Synch until TXE is dropped. Note that transmission is not aborted on loss of carrier.
FU	D5	**FIFO UNDERRUN**: Set when ENC cannot gain access of the bus before the FIFO empties. Transmission of the packet will be aborted.
CDH	D6	**CD HEARTBEAT**: Set when the transceiver fails to issue a collision signal after transmission of a packet. The Collision Detect (CD) heartbeat signal must commence during the first 6.4μs of the Interframe Gap following a transmission. However, in some collisions, the CD heartbeat bit will be set even when the transceiver is not performing the CD heartbeat test.
OWC	D7	**OUT-OF-WINDOW COLLISION**: Set when a collision occurred after a slot time (51.2μs). Transmission will not be aborted.

REGISTER DESCRIPTION (Continued)

G. RECEIVE CONFIGURATION REGISTER (RCR) 0CH (WRITE)

This register determines what types of packets to be accepted and what mode the ENC will be in. The types include address type and error type. In the error type, when any one bit of SEP and AR is clear and the packet received matches the condition set in SEP or AR, the packet is rejected.



SYMBOL	BIT	DESCRIPTION
SEP	D0	**SAVE ERROR PACKETS.** 0: Packets with CRC and Frame Alignment errors are rejected. 1: Packets with CRC and Frame Alignment errors are accepted.
AR	D1	**ACCEPT RUNT PACKETS**: This bit allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt. 0: Packets with fewer than 64 bytes rejected. 1: Packets with fewer than 64 bytes accepted.
AB	D2	**ACCEPT BROADCAST**: Enables the receiver to accept a packet with an all 1's destination address. 0: Packets with broadcast destination address rejected. 1: Packets with broadcast destination address accepted.
AM	D3	**ACCEPT MULTICAST**: Enables the receiver to accept a packet with a multicast address; all multicast addresses must pass the hashing array. 0: Packets with multicast destination address not checked. 1: Packets with multicast destination address checked.

REGISTER DESCRIPTION (Continued)

G. RECEIVE CONFIGURATION REGISTER (RCR) 0CH (WRITE)

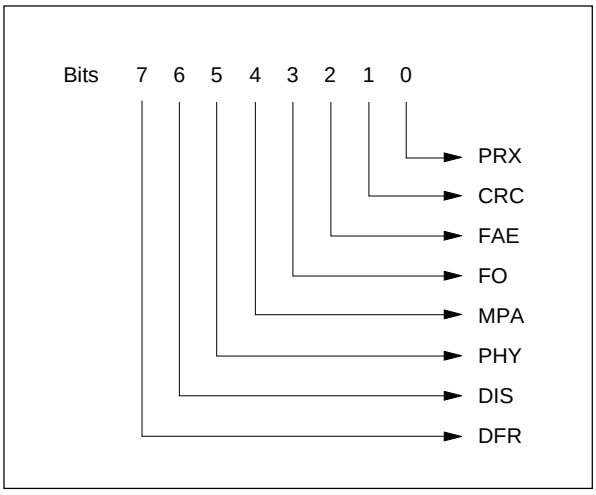
SYMBOL	BIT	DESCRIPTION
PRO	D4	**PROMISCUOUS PHYSICAL:** Enables the receiver to accept all packets with a physical address. 0: Physical address of mode must match the station address programmed in PAR0-PAR5. 1: All packets with physical addresses accepted.
MON	D5	**MONITOR MODE**: Enables the receiver to check addresses and CRC on incoming packets without buffering to memory. The Missed Packet Tally Counter will be incremented for each recognized packet. 0: Packets buffered to memory. 1: Packets checked for address match, good CRC and frame alignment but not buffered to memory.
RESERVED	D6	**Reserved**
RESERVED	D7	**Reserved**

Note: D2 and D3 are "OR'd" together, i.e., if D2 and D3 are set the ENC will accept broadcast and multicast addresses as well as its own physical address. To establish full promiscuous mode, bits D2, D3 and D4 should be set. In addition, the multicast hashing array must be set to all 1's in order to accept all multicast addresses.

REGISTER DESCRIPTION (Continued)

H. RECEIVE STATUS REGISTER (RSR) 0CH (READ)

This register records status of the received packet. It includes information on errors, the type of address match, either physical or multicast, and the aborted packet type. The contents of this register are written to buffer memory by the DMA after receiving a good packet. If packets with errors are to be saved the receive status is written to memory at the head of the erroneous packet, when an erroneous packet is received. If packets with errors are to be rejected the RSR will not be written to memory. The contents will be cleared when the next packet arrives. CRC errors, frame alignment errors and missed packets are counted internally by the ENC which relinquishes the host from reading the RSR in real time to record errors for Network Management Functions. The contents of this register are not specified until after the first reception.



SYMBOL	BIT	DESCRIPTION
PRX	D0	**PACKET RECEIVED CORRECTLY**: Indicates Packet received without error. (Bits CRC, FAE, FO and MPA are zero for the received packet.) Set when packets are received complete.
CRC	D1	**CRC ERROR**: Indicates packet received with CRC error. Increments Tally Counter (CNTR1). This bit will also be set for Frame Alignment errors. Set when packets are received complete.
FAE	D2	**FRAME ALIGNMENT ERROR**: Indicates that the incoming packet did not end on a byte boundary and the CRC did not match at last byte boundary. Increments Tally Counter (CNTR0). Set when packets are received complete.
FO	D3	**FIFO OVERRUN:** This bit is set when the FIFO is not serviced causing overflow during reception. Reception of the packet will be aborted.
MPA	D4	**MISSED PACKET**: Set when packet intended for node cannot be accepted by ENC because of a lack of receive buffers, or if the controller is in monitor mode and did not buffer the packet to memory increments Tally Counter (CNTR2).

REGISTER DESCRIPTION (Continued)

H. RECEIVE STATUS REGISTER (RSR) 0CH (READ) (Continued)

SYMBOL	BIT	DESCRIPTION
PHY	D5	**PHYSICAL/MULTICAST ADDRESS**: Indicates whether received packet has a physical or multicast address type. Set/reset when Destination Address has been received. 0: Physical Address Match 1: Multicast/ Broadcast Address Match
DIS	D6	**RECEIVER DISABLED:** Set when receiver is disabled by entering Monitor mode. Reset when receiver is re-enabled when exiting the Monitor mode.
DFR	D7	**DEFERRING**: Set when CRS or COL inputs are active. If the transceiver has asserted the CD line as a result of the jabber, this bit will stay set indicating the jabber condition.

Note: The following coding applies to CRC and FAE bits

FAE	CRC	Type of Error
0	0	No Error (Good CRC and < 5 Dribble Bits)
0	1	CRC Error
1	0	Illegal, will not occur
1	1	Frame Alignment Error and CRC Error

REGISTER DESCRIPTION
I. REGISTER ADDRESS ASSIGNMENTS (Continued)

PAGE 0 ADDRESS ASSIGNMENTS (PS1 = 0, PS0 = 0)

RA3-RA0	READ	WRITE
00H	Command Register (CR)	Command Register (CR)
01H	Current Local DMA Address 0 (CLDA0)	Page Start Register (PSTART)
02H	Current Local DMA Address 1 (CLDA1)	Page Stop Register (PSTOP)
03H	Boundary Pointer (BNRY)	Boundary Pointer (BNRY)
04H	Transmit Status Register (TSR)	Transmit Page Start Address (TPSR)
05H	Number of Collisions Register (NCR)	Transmit Byte Count Register 0 (TBCR0)
06H	FIFO (FIFO)	Transmit Byte Count Register 1 (TBCR1)
07H	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
08H	Current Remote DMA Address 0 (CRDA0)	Remote Start Address Register 0 (RSAR0)
09H	Current Remote DMA Address 1 (CRDA1)	Remote Start Address Register 1 (RSAR1)
0AH	Reserved	Remote Byte Count Register 0 (RBCR0)
0BH	Reserved	Remote Byte Count Register 1 (RBCR1)
0CH	Receive Status Register (RSR)	Receive Configuration Register (RCR)
0DH	Tally Counter 0 (Frame Alignment Error) (CNTR0)	Transmit Configuration Register (TCR)
0EH	Tally Counter 1 (CRC Error) (CNTR1)	Data Configuration Register (DCR)
0FH	Tally Counter 2 (Missed Packet Error) (ENTR2)	Interrupt Mask Register (IMR)

REGISTER DESCRIPTION (Continued)
I. REGISTER ADDRESS ASSIGNMENTS (Continued)

PAGE 1 ADDRESS ASSIGNMENTS (PS1 = 0, PS0 = 1)

RA3-RA0	READ	WRITE
00H	Command Register (CR)	Command Register (CR)
01H	Physical Address Register 0 (PAR0)	Physical Address Register 0 (PAR0)
02H	Physical Address Register 1 (PAR1)	Physical Address Register 1 (PAR1)
03H	Physical Address Register 2 (PAR2)	Physical Address Register 2 (PAR2)
04H	Physical Address Register 3 (PAR3)	Physical Address Register 3 (PAR3)
05H	Physical Address Register 4 (PAR4)	Physical Address Register 4 (PAR4)
06H	Physical Address Register 5 (PAR5)	Physical Address Register 5 (PAR5)
07H	Current Page Register (CURR)	Cruuent Page Register (CURR)
08H	Multicast Address Register 0 (MAR0)	Multicast Address Register 0 (MAR0)
09H	Multicast Address Register 1 (MAR1)	Multicast Address Register 1 (MAR1)
0AH	Multicast Address Register 2 (MAR2)	Multicast Address Register 2 (MAR2)
0BH	Multicast Address Register 3 (MAR3)	Multicast Address Register 3 (MAR3)
0CH	Multicast Address Register 4 (MAR4)	Multicast Address Register 4 (MAR4)
0DH	Multicast Address Register 5 (MAR5)	Multicast Address Register 5 (MAR5)
0EH	Multicast Address Register 6 (MAR6)	Multicast Address Register 6 (MAR6)
0FH	Multicast Address Register 7 (MAR7)	Multicast Address Register 7 (MAR7)

REGISTER DESCRIPTION (Continued)

I. REGISTER ADDRESS ASSIGNMENTS

PAGE 2 ADDRESS ASSIGNMENTS (PS1 = 1, PS0 = 0)

RA3-RA0	READ	WRITE
00H	Command Register (CR)	Command Register (CR)
01H	Page Start Register (PSTART)	Current Local DMA Address 0 (CLDA0)
02H	Page Start Register (PSTOP)	Current Local DMA Address 1 (CLDA1)
03H	Remote Next Packet Pointer	Remote Next Packet Pointer
04H	Transmit Page Start Address (TPSR)	Reserved
05H	Local Next Packet Pointer	Local Next Packet Pointer
06H	Address Counter (Upper) (ACU)	Address Counter (Upper) (ACU)
07H	Address Counter (Lower) (ACL)	Address Counter (Lower) (ACL)
08H	Reserved	Reserved
09H	Reserved	Reserved
0AH	Reserved	Reserved
0BH	Reserved	Reserved
0CH	Receive Configuration Register (RCR)	Reserved
0DH	Transmit Configuration Register (TCR)	Reserved
0EH	Data Configuration Register (DCR)	Reserved
0FH	Interrupt Mask Register (IMR)	Reserved

Note: Page 2 registers should only be accessed for diagnostic purposes. They should not be modified during normal operation.
Page 3 should never be modified.

REGISTER DESCRIPTION (Continued)

J. DMA REGISTERS

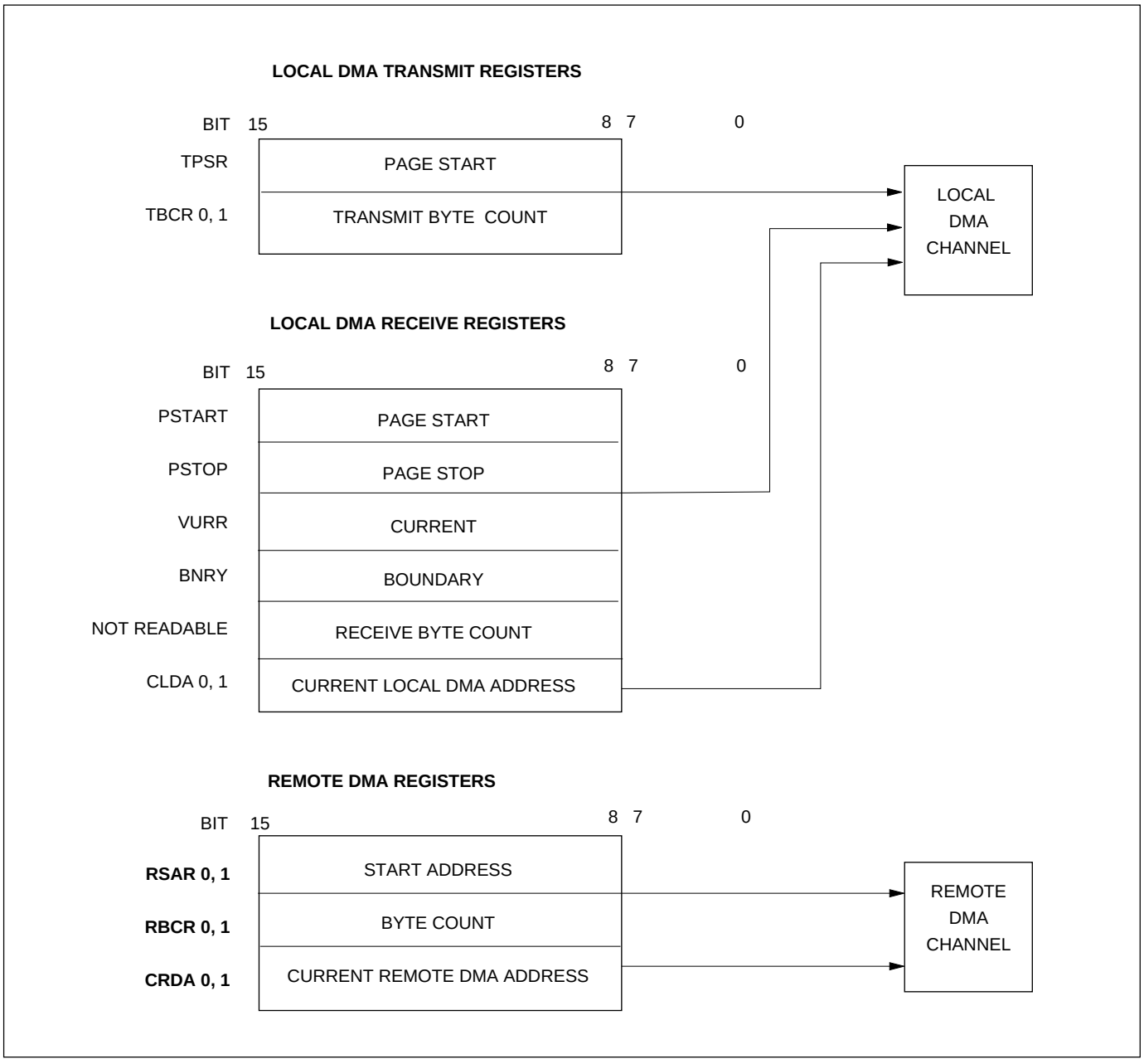
The DMA Registers are partitioned into three groups: Transmit, Receive, and Remote DMA Registers, as the diagram show on the next page.

The Transmit group contains three registers: TPSR, TBCR0 and TBCR1. Registers in this group are used to initialize the Local DMA Channel for transmission of packets.

PSTART, PSTOP, CURR, BNRY, Receive Byte Counter, CLDA0 and CLDA1 are located in the receive group. They are used to initialize the Local DMA Channel for packet reception. Meanwhile, the Page Start, Page Stop, Current and Boundary Registers are also used by the Buffer Management Logic to supervise the Receive Buffer Ring.

The Remote DMA Registers are used to initialize the Remote DMA. Six registers are included: RSAR0, RSAR1, RBCR0, RBCR1, CRDA0 and CRDA1.

The diagram on the next page shows 8- and 16-bit registers. For slave mode read/write, the 16-bit internal registers are also accessed as 8-bit registers by the host. Thus, the 16-bit Transmit Byte Count Register is broken into two 8-bit registers, namely, TBCR0 and TBCR1. Similarly, Remote Start Address and Remote Byte Count are broken into RSAR0, RSAR1, and RBCR0, RBCR1. Registers TPSR, PSTART, PSTOP, CURR and BNRY only check or control the upper 8 bits of address information on the bus. Thus, they are shifted to position 15-8, as shown in the diagram on the next page.


LOCAL DMA TRANSMIT REGISTERS
BIT 15
8 7
0
TPSR
PAGE START
TBCR 0, 1
TRANSMIT BYTE COUNT
LOCAL DMA CHANNEL
LOCAL DMA RECEIVE REGISTERS
BIT 15
8 7
0
PSTART
PAGE START
PSTOP
PAGE STOP
VURR
CURRENT
BNRY
BOUNDARY
NOT READABLE
RECEIVE BYTE COUNT
CLDA 0, 1
CURRENT LOCAL DMA ADDRESS
REMOTE DMA REGISTERS
BIT 15
8 7
0
RSAR 0, 1
START ADDRESS
RBCR 0, 1
BYTE COUNT
CRDA 0, 1
CURRENT REMOTE DMA ADDRESS
REMOTE DMA CHANNEL

REGISTER DESCRIPTION (Continued)
J. DMA REGISTERS (Continued)

TRANSMIT DMA REGISTER (TPSR)

This register points to the page where the assembled packet is ready to be transmitted. Only the eight higher order addresses are specified since all transmit packets are assembled on 256-byte page boundaries. The bit assignment is shown below. The values placed in bits D7-D0 will be used to initialize the higher order address (A15-A8) of the Local DMA for transmission while the lower order bits (A7-A0) are initialized to zero.

BIT ASSIGNMENT

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TPSR	A15	A14	A13	A12	A11	A10	A9	A8

(A7-A0 initialized to zero)

TRANSMIT BYTE COUNT REGISTER 0, 1 (TBCR0, 1)

These two registers indicate the length of the packet to be transmitted in bytes. The count must include the number of bytes in the source, destination, length and data fields (CRC field is exclusive). The maximum number of transmit bytes allowed is 64 kbytes. The ENC will not truncate transmissions whenever packet length is longer than 1500 bytes. Hence, in order to meet the IEEE 802.3 standard, software driver on upper layer must take care of maximum length problem by itself. The bit assignment is shown below:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBCR1	L15	L14	L13	L12	L11	L10	L9	L8

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBCR0	L7	L6	L5	L4	L3	L2	L1	L0

REGISTER DESCRIPTION (Continued)
J. DMA REGISTERS (Continued)

LOCAL DMA RECEIVE REGISTERS

PAGE START/STOP REGISTERS (PSTART, PSTOP)

The Page Start and Stop Registers program the starting and stopping page address of the Receive Buffer Ring. Since the ENC uses fixed 256-byte buffers aligned on page boundaries, only the upper eight bits of the start and stop address are specified.

PSTART, PSTOP bit assignment.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSTART,								
PSTOP	A15	A14	A13	A12	A11	A10	A9	A8

BOUNDARY REGISTER (BNRY)

This register is used to prevent overflow of the Receive Buffer Ring. Buffer Management compares the contents of this register to the next buffer address when linking buffers together. If the contents of this register match the next buffer address, the Local DMA operation is aborted and the corresponding bit in ISR will be set.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BNRY	A15	A14	A13	A12	A11	A10	A9	A8

7 6 5 4 3 2 1 0

BARY A15 A14 A13 A12 A11 A10 A9 A8

CURRENT PAGE REGISTER (CURR)

This register is used internally by the buffer management logic as a backup register for reception. CURR contains the address of the first buffer to be used for a packet reception, and is used to restore DMA pointers if receive errors occur. This register is initialized to the same value as PSTART, and should not be written to unless the controller is reset.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CURR	A15	A14	A13	A12	A11	A10	A9	A8

REGISTER DESCRIPTION (Continued)

J. DMA REGISTERS

CURRENT LOCAL DMA REGISTER 0, 1 (CLDA0, 1)
CURRENT PAGE REGISTER (CURR)

The temporary local DMA address will be stored in these two registers after each burst transfer is completed. When another burst transfer is ready to start, values within these two registers will be loaded into the Address Counters (ACU and AQL) as the address for local DMA channel.

This register is used internally by the Buffer Management Logic as a backup registers for reception. Curr contains the address of the first buffer to be used for a packet reception, and is used to restore DMA pointers if receive errors occur. This register is initialized to the same value as PSTART, and should not be written to again unless the controller is reset.

These two registers can be accessed to determine the current local DMA address.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CURR	A15	A14	A13	A12	A11	A10	A9	A8
CLDA1	A15	A14	A13	A12	A11	A10	A9	A8

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLDA0	A7	A6	A5	A4	A3	A2	A1	A0

REMOTE DMA REGISTER

REMOTE START ADDRESS REGISTERS (RSAR0, 1)

Remote DMA operations are programmed through the Remote Start Address (PSAR0, 1) and Remote Byte Count (RBCR0, 1) registers. The Remote Start Address is used to point to the start of the block of data to be transferred, while the Remote Byte Count is used to indicate the length of the block (in bytes)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSAR1	A15	A14	A13	A12	A11	A10	A9	A8

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSAR0	A7	A6	A5	A4	A3	A2	A1	A0

REGISTER DESCRIPTION (Continued)
J. DMA REGISTER (Continued)

REMOTE BYTE COUNT REGISTERS (RBCR0, 1)
REMOTE DMA REGISTER

REMOTE START ADDRESS REGISTERS (RSAR0, 1)

Remote DMA operations are programmed through the Remote Start Address (PSAR0, 1) and Remote Byte Count (PBCR0, 1) registers. The Remote Start Address is used to point to the start of the block of data to be transferred, while the Remote Byte Count is used to indicate the length of the block (in bytes)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBCR1	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBCR0	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0

Note:
- RSAR1 programs the start address bits A8-A15
- RSAR0 programs the start address bits A0-A7
- Address incremented by two for word transfers, and by one for byte transfers
- RBCR1 programs MSB byte count
- RBCR0 programs LSB byte count
- Byte count decremented by two for word transfers, and by one for byte transfers

CURRENT REMOTE DMA ADDRESS (CRDA0, 1)

The Current Remote DMA Registers contain the current address of the Remote DMA. CRDA1/0 are similar to CLDA1/0 except that CRDA1/0 store the temporary address of the Remote DMA. The bit assignment is shown below:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRDA1	A15	A14	A13	A12	A11	A10	A9	A8

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRDA0	A7	A6	A5	A4	A3	A2	A1	A0

REGISTER DESCRIPTION (Continued)

J.. DMA REGISTER (Continued)

FIFO

CURRENT REMOTE DMA ADDRESS (CRDA0, 1)

This is an 8-bit register which allows the CPU to examine the contents of the FIFO after loopback. The FIFO will contain the last 8 data bytes transmitted in the loopback packet. Sequential reads from the FIFO will advance a pointer in the FIFO automatically and reading of all 8 bytes.

The Current Remote DMA Registers contain the current address of the Remote DMA. CRDA1/0 are similar to CLDA1/0 except that CRDA1/0 store the temporary address of the Remote DMA. The bit assignment is shown below:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Note: The FIFO should only be read when the ENC has been programmed in the loopback mode.