7. DC Parameters

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
VDD	Supply voltage	VSS-0.3	VSS+7.0	V	1
Vip	Voltage applied to any pin	VSS-0.3	VDD+0.3	V	1
Ts	Storage temperature	-40	125	deg.C	1

NOTE:

(1) These are stress ratings only. Exceeding the absolute maximum ratings may permanantly damage the device. Operating the device at absolute maximum ratings for extended periods may affect device reliability.

7.2 DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
VDD	Supply voltage	4.75	5.00	5.25	V	1
Vihc	IC input HIGH voltage	3.5		VDD	V	1,2
Vilc	IC input LOW voltage	0.0		0.8	V	1,2
Ta	Ambient operating temperature	0		70	deg.C	

NOTES:

(1) Voltages measured with respect to VSS.

(2) IC - CMOS compatible inputs.

7.3 DC Characteristics

KEY
Mes - Values measured from a sample MEMC.
Nom - Nominal values derived from analogue simulations.

Symbol	Parameter	Mes	Nom	Units	Note
IDD	Supply current			mA	
|Isc|	Output short circuit current	>25		mA	1
|Ilu|	D.C. latch-up current	300		mA	2
|Iinc|	IC input leakage current		10	uA	
Vohc	OC output HIGH voltage		4.2	V	3,6
Volc	OC output LOW voltage		0.3	V	3,7
Voht	OT output HIGH voltage		3.7	V	4,8
Volt	OT output LOW voltage		0.4	V	4,9
Vihct	IC input HIGH voltage threshold		2.8	V	5
Vilct	IC input LOW voltage threshold		2.0	V	5
Cin	Input capacitance	5		pF	

NOTES:

(1) Not more than one output should be shorted to either rail at any time, and for no longer than 1 second.

(2) This value represents the D.C. current that the input/output pins can tolerate before the chip latches up.

(3) OC - CMOS compatible outputs.

(4) OT - TTL compatible outputs.

(5) IC - CMOS compatible inputs.

(6) Output current = 3mA

(7) Output current = -3mA

(8) Output current = 10mA

(9) Output current = -10mA

8. AC Parameters

TEST CONDITIONS

The AC timing diagrams presented in this section assume that the outputs of MEMC have been loaded with the capacitive loads shown in the 'Test Load' column of Table 3; these loads have been chosen as typical of the type of system in which MEMC will be employed.

The output pads of MEMC are CMOS drivers which exhibit a propagation delay that increases linearly with the increase in load capacitance. An 'Output derating' figure is given for each output pad, showing the approximate increase in load capacitance necessary to increase the output time by one nanosecond.

Output Signal	Test Load (pF)	Output derating (pF/ns)	Note
PH1	15	5	1
PH2	15	5	1
DBE	20	5	
ABORT	10	5	
$\overline{\text{IORQ}}$	10	5	
REF8M	20	5	
RA[0:9]	250	8	
$\overline{\text{RAS}}$	250	8	
$\overline{\text{CAS}}$[0:3]	60	8	
$\overline{\text{ROMCS}}$	40	5	
$\overline{\text{VIDW}}$	10	5	
$\overline{\text{VIDAK}}$	10	5	
$\overline{\text{SNDAK}}$	10	5	
$\overline{\text{SIRQ}}$	10	5	

(1) To maintain **PH1/PH2** non-overlap, the capacitive load on **PH1** and **PH2** should not exceed 25pF.

Table 3: AC test loads

KEY TO TIMING TABLES

Sym - Symbol used in the timing diagrams.

Mes - Times measured in a sample ARM/MEMC/VIDC/IOC system running at 8MHz.

Nom - Nominal times.

Lim - Times required to meet ARM/MEMC/VIDC/IOC system specifications.

8.1 Input Clock

```
                 ___________________________
                |                           |                           |
CK24M   ___     |                           |___________________________|
                |                           |                           |
                |<---------- t1 ----------->|<---------- t2 ----------->|
```

8.2 Processor Signals

```
                  ___ //____
                     //      |                                  ____
PH2                          |___________ //___________|
                             |                //
                             |
                       ->|   |<- t3                   ->|   |<- t4
                    __   |__ |_____________ //___________|__|  __
                      \/     |               //             |   \/
A[0:25]             __/\___ |___________ //_____________|___/\__
                             |               //
                       ->|   |<- t5                   ->|   |<- t6
                    __   |__ |_____________ //___________|__|  __
                      \/     |               //             |   \/
R/W                 __/\___ |___________ //_____________|___/\__
                             |               //
                       ->|   |<- t7                   ->|   |<- t8
                    __   |__ |_____________ //___________|__|  __
                      \/     |               //             |   \/
B/W                 __/\___ |___________ //_____________|___/\__
                             |               //
                       ->|   |<- t9                   ->|   |<- t10
                    __   |__ |_____________ //___________|__|  __
                      \/     |               //             |   \/
SPVMD               __/\___ |___________ //_____________|___/\__
                             |               //
                |<---- t11 --->|  |<- t12
             __ |_____________|__|  __
               \/              |   \/
MREQ         __/\_____________|___/\__
                             |
                |<---- t13 --->|  |<- t14
             __ |_____________|__|  __
               \/              |   \/
SEQ          __/\_____________|___/\__
                             |
```

Sym	Parameter	Mes	Nom	Lim	Units	Note
t1	CK24M input clock HIGH	22	21		ns	
t2	CK24M input clock LOW	20	21		ns	

Sym	Parameter	Mes	Nom	Lim	Units	Note
t3	A[0:25] Address setup	0	0		ns	
t4	A[0:25] Address hold	27	0		ns	
t5	$\overline{R}$/W setup	0	0		ns	
t6	$\overline{R}$/W hold	33	0		ns	
t7	$\overline{B}$/W setup	24	0		ns	
t8	$\overline{B}$/W hold	23	0		ns	
t9	SPVMD setup		0		ns	1
t10	SPVMD hold		0		ns	1
t11	$\overline{MREQ}$ setup	100	75		ns	
t12	$\overline{MREQ}$ hold	23	0		ns	
t13	SEQ setup	70	75		ns	
t14	SEQ hold	28	0		ns	

NOTE:

(1) Transitions on **SPVMD** should normally occur only while **PH2** is HIGH. If **SPVMD** changes during the **PH2** LOW period of an access to a protected area of memory (including protected Logical pages), the access may not be allowed or aborted as expected.

8.3 Processor Controls

```
                 ________ //_________                                  ___
                |        //           |                               |
PH1   _________|                      |______________ //____________|
                |                      |                //
         ->| |<- t15              ->| |<- t16
      ______|                         |____________ //__________
                |                      |                //          |
PH2             |___________ //_______|                            |___
                |           //        |                            |
                |                     |                            |
                |<--------- t17 ---------->|<-------- t18 --------->|
                |                     |                            |
                |<-t19->|             |                  t20 ->| |<-
      ______|_      |_______________|_________________________|_|
DBE             | \/\/\/                                      | \/\/
      ______|_/\/\/\_____________________________________|_/\/\
                |                     |                            |
                          |<--- t21 -->|  |<- t22
                       __ |____________|__|  __
                         \/                 \/
ABORT                  __/\_______________/\__
                                |
```

Sym	Parameter	Mes	Nom	Lim	Units	Note
t15	PH2 to PH1 non-overlap	9	10	> 0	ns	1
t16	PH1 to PH2 non-overlap	9	10	> 0	ns	1
t17	PH2 LOW period	196	187		ns	2
t18	PH2 HIGH period	54	62		ns	2
t19	PH2 LOW to DBE valid	5	0		ns	
t20	PH2 LOW to DBE invalid	5	0		ns	
t21	ABORT to PH2 setup		80	> 35	ns	3
t22	ABORT to PH2 hold		10	> 0	ns	3

NOTES:

(1) The ARM processor clocks must never overlap.

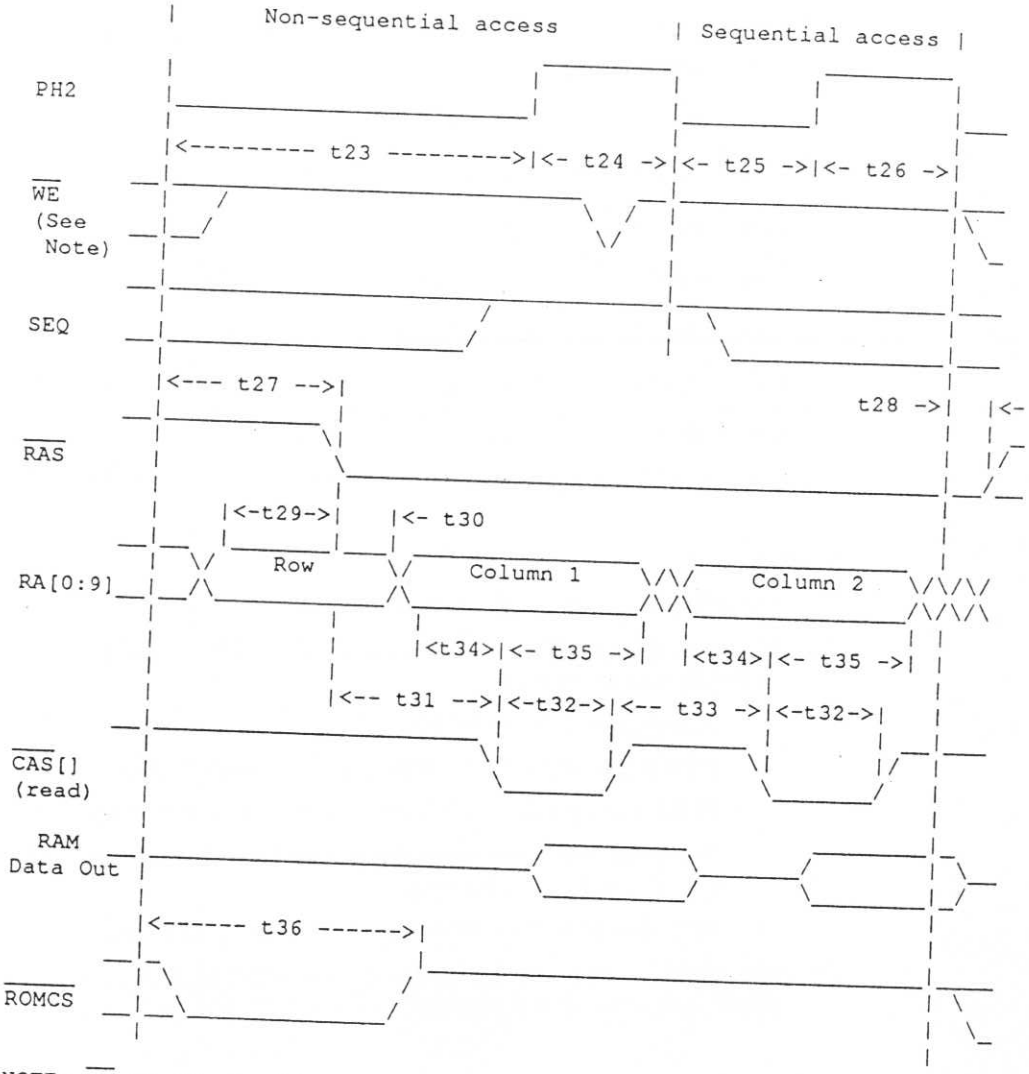
(2) Most processor cycles take 250ns, with **PH2** LOW for 187ns and HIGH for 62ns. The following exceptions apply:

- Processor internal cycles take 125nS.
- DRAM and nibble-mode ROM S-cycle memory accesses take 125ns.
- ROM read operation cycle time is selectable, and may take 250ns, 375ns or 500ns.
- The processor clocks are suspended during I/O cycles, with **PH2** being held HIGH until the end of the I/O cycle.
- **PH2** may be held LOW during DMA and refresh operations.

(3) The **ABORT** setup and hold limits for the ARM processor were measured for a sample ARM. A factor of two should be allowed for process variations.

8.4 Processor accessing Dynamic RAM

8.4.1 Processor - Dynamic RAM read cycles



NOTE: $\overline{WE}$ is obtained by passing DBE through an external inverter.

Sym	Parameter	Mes	Nom	Lim	Units	Note
t23	DRAM N-cycle:PH2 LOW	196	187		ns	
t24	DRAM N-cycle:PH2 HIGH	54	62		ns	
t25	DRAM S-cycle:PH2 LOW	71	62		ns	
t26	DRAM S-cycle:PH2 HIGH	54	62		ns	
t27	$\overline{RAS}$ enable time	110	105		ns	
t28	$\overline{RAS}$ disable time	8	0		ns	
t29	Row Address setup	93	40	> 0	ns	1
t30	Row Address hold	26	20	> 15	ns	1
t31	$\overline{RAS}$ to $\overline{CAS}$[] enable (read)	58	62	> 25	ns	1
t32	$\overline{CAS}$[] pulse width (read)	63	62	> 60	ns	1
t33	$\overline{CAS}$[] precharge period (read)	60	62	> 50	ns	1
t34	Column Address setup (read)	13	20	> 0	ns	1
t35	Column Address hold (read)	89	62	> 20	ns	1
t36	$\overline{ROMCS}$ disable time (read cycle)	130	125		ns	

NOTE:

(1) The DRAM timing limits are given for the particular DRAM used in the test system.

8.4.2 Processor - Dynamic RAM write cycles

```
                 |        Non-sequential access        | Sequential access |
                 |                                     |                   |
PH2              |                                     |                   |
                 |<--------- t23 --------->|<- t24 ->|<- t25 ->|<- t26 ->|
WE               |                                     |                   |
(See             |                                     |                   |
 Note)           |                                     |                   |
                 |                                     |                   |
SEQ              |                                     |                   |
                 |<--- t27 -->|                                  t28 ->|   |<-
                 |            |                                        |   |
RAS              |            |                                        |   |
                 |<-t29->|    |<- t30                                  |
                 |       |    |                                        |
                 |   Row     |    Column 1     |    Column 2           |
RA[0:9]          |                                                     |
                 |            |<- t40 ->|<t41>|  |<- t40 ->|<t41>|     |
                 |            |<---- t37 ---->|<-t38->|<-- t39 ->|<-t38->|
CAS[]            |                                                     |
(write)          |                                                     |
                 |                                                     |
  RAM            |                                                     |
Data in          |                                                     |
                 |                                                     |
              ->|    |<- t42                                          |
                 |                                                     |
ROMCS            |                                                     |
```

NOTE: $\overline{WE}$ is obtained by passing DBE through an external inverter.

Sym	Parameter	Mes	Nom	Lim	Units	Note
t23	DRAM N-cycle:PH2 LOW	196	187		ns	
t24	DRAM N-cycle:PH2 HIGH	54	62		ns	
t25	DRAM S-cycle:PH2 LOW	71	62		ns	
t26	DRAM S-cycle:PH2 HIGH	54	62		ns	
t27	$\overline{RAS}$ enable time	110	105		ns	
t28	$\overline{RAS}$ disable time	8	0		ns	
t29	Row Address setup	93	40	> 0	ns	1
t30	Row Address hold	26	20	> 15	ns	1
t37	$\overline{RAS}$ to $\overline{CAS}$[] enable (write)	79	83	> 25	ns	1
t38	$\overline{CAS}$[] pulse width (write)	63	62	> 60	ns	1
t39	$\overline{CAS}$[] precharge period (write)	60	62	> 25	ns	1
t40	Column Address setup (write)	34	40	> 0	ns	1
t41	Column Address hold (write)	68	40	> 20	ns	1
t42	$\overline{ROMCS}$ disable time (write cycle)	5	0		ns	

NOTE:

(1) The DRAM timing limits are given for the particular DRAM used in the test system.

8.5 Processor accessing ROM

8.5.1 Non-sequential ROM access

```
        ___
           |                                  _______________
PH2        |_______________ //_______________|               |
           |               //                |               |_________
           |                                 |               |
           |<----------- t43 -------------->|<----- t44 ---->|
           |                                 |               |
           |<- t45 ->|                       |               |<-t42->|
        ___|_______  |                       |               |       |
           |       \ |                       |               |       | /_
ROMCS   ___|_______\|_______________________|_______________|_______|/__
           |        |                       |               |       |
```

8.5.2 Sequential ROM access (only with 200ns/60ns nibble-mode ROMs)

```
           |      Non-sequential          | Sequential  |   Non-ROM
           |          access              |   access    |    access
        ___                        _______        _______
           |                       |       |      |       |
PH2        |_______________________|       |______|       |_______________
           |                       |       |      |       |
           |<------- t46 ------->|<-t47->|<-t48->|<-t49->|
           |                                |             |
        __|_______________________________|__           |
           |                   /            |  \          |
SEQ     __|_________________/              |   \_________|_______________
           |                                             |
        ->|    |<- t45                                  |<-- t42 -->|
        __|__  |                                         |           | _
           |  \ |                                         |           | /
ROMCS   __|___\|_________________________________________|___________|/__
           |
```

Sym	Parameter	Mes	Nom	Lim	Units	Note
t42	$\overline{\text{ROMCS}}$ disable time	5	0		ns	
t43	200ns ROM read:PH2 LOW	196	187		ns	1
	325ns ROM read:PH2 LOW	320	312		ns	1
	450ns ROM read:PH2 LOW	445	437		ns	1
t44	All ROM reads: PH2 HIGH	54	62		ns	
t45	$\overline{\text{ROMCS}}$ enable time	5	0		ns	
t46	200/60ns ROM N-cycle:PH2 LOW	196	187		ns	
t47	200/60ns ROM N-cycle:PH2 HIGH	54	62		ns	
t48	200/60ns ROM S-cycle:PH2 LOW	71	62		ns	
t49	200/60ns ROM S-cycle:PH2 HIGH	54	62		ns	

NOTE:

(1) The basic ROM access time is selectable as 200ns, 325ns or 450ns. **PH2** is held LOW to extend the processor cycle, resulting in processor cycle times of 250ns, 375ns and 500ns respectively.

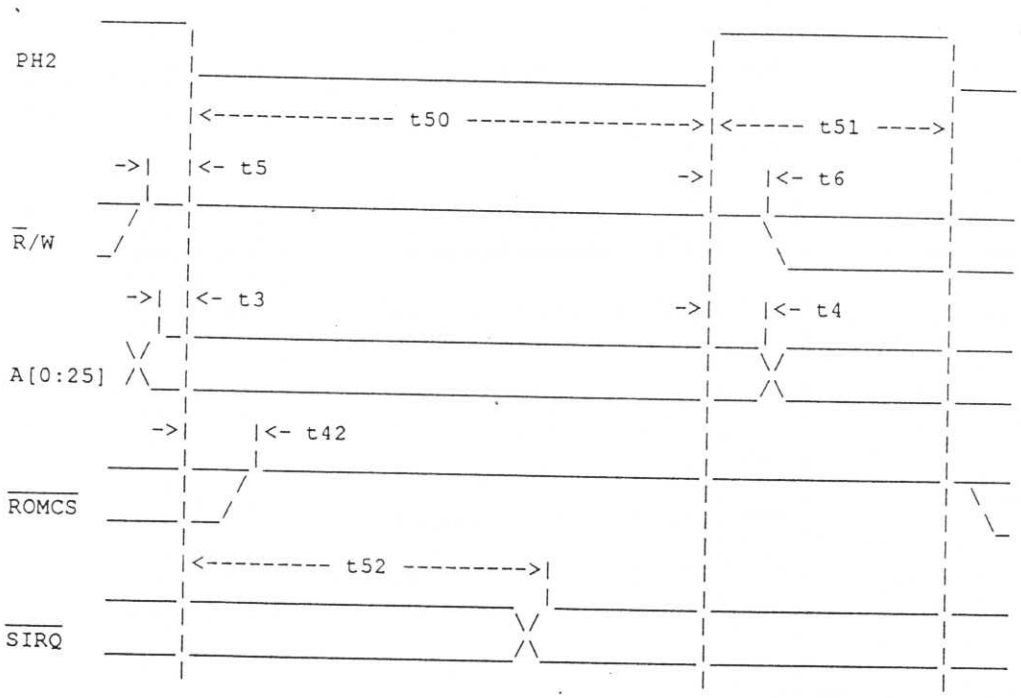
8.6 Processor accessing MEMC Internal Blocks

This timing diagram applies when the processor is writing to:

(i) Logical to Physical Address Translator

(ii) DMA Address Generators

(iii) MEMC Control Register



Sym	Parameter	Mes	Nom	Lim	Units	Note
t3	A[0:25] Address setup	0	0		ns	
t4	A[0:25] Address hold	27	0		ns	
t5	$\overline{R}$/W setup	0	0		ns	
t6	$\overline{R}$/W hold	33	0		ns	
t42	$\overline{ROMCS}$ disable time (write cycle)	5	0		ns	
t50	MEMC write: PH2 LOW	196	187		ns	
t51	MEMC write: PH2 HIGH	54	62		ns	
t52	$\overline{SIRQ}$ enable/disable time		150		ns	1

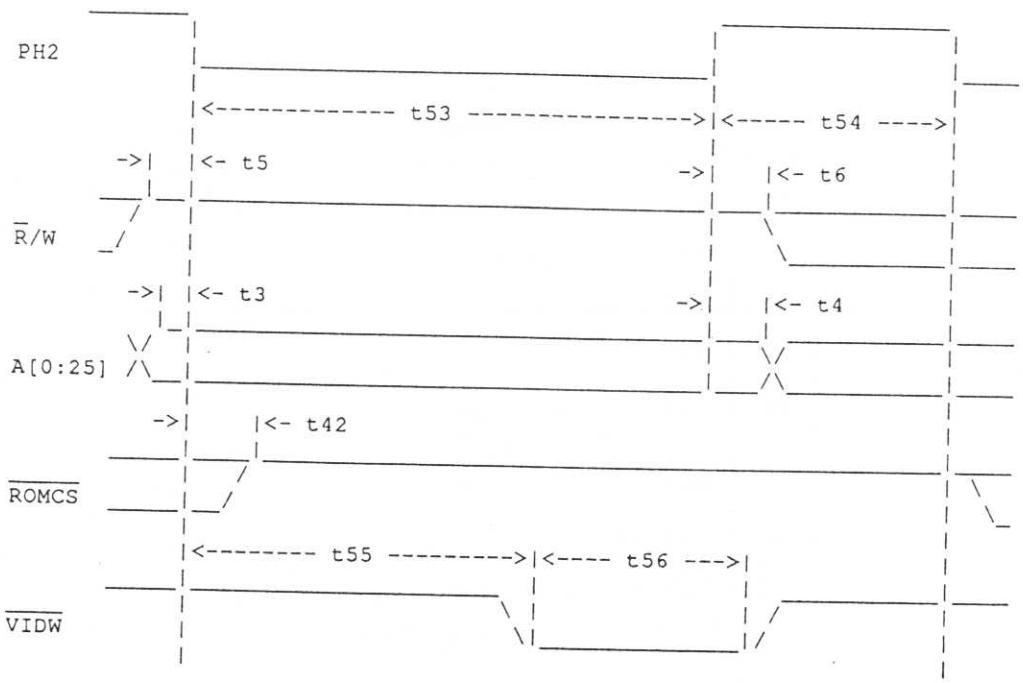
NOTE:

(1) The $\overline{SIRQ}$ interrupt is affected under the following circumstances:

- The $\overline{SIRQ}$ line is driven HIGH when the *DMA Address Generator* 'Sstart' register is programmed.
- The $\overline{SIRQ}$ line is driven LOW when the *DMA Address Generator* 'Sptr' register is programmed.

8.7 Processor accessing the Video Controller

This timing diagram applies when the processor performs a write operation to the Video Controller area of the memory map.



Sym	Parameter	Mes	Nom	Lim	Units	Note
t3	A[0:25] Address setup	0	0		ns	
t4	A[0:25] Address hold	27	0		ns	
t5	$\overline{R}$/W setup	0	0		ns	
t6	$\overline{R}$/W hold	33	0		ns	
t42	$\overline{ROMCS}$ disable time (write cycle)	5	0		ns	
t53	Video Controller write : PH2 LOW	196	187		ns	
t54	Video Controller write : PH2 HIGH	54	62		ns	
t55	PH2 LOW to $\overline{VIDW}$ enable		125		ns	
t56	$\overline{VIDW}$ pulse width	83	83	> 20	ns	1

NOTE:

(1) The **VIDW** pulse width limit was measured for a sample VIDC. A factor of two should be allowed for process variations.

8.8 Direct Memory Access (DMA) operations

8.8.1 DMA operation

```
                |     N-cycle       | S-cycle   | S-cycle   | S-cycle   |
                |                   |           |           |           |

                |                   |  ___________________________________|__
                |                   | /         /|                        |
 ____ ____      |                   |/_________/ |                        |
VIDRQ,SNDRQ_|___________________|                |                        |
                |                   |            |                        |
                |                   |<-- t58 -->|                        |
              _|___________________|      ____       ____       ____      |__
 ____ ____      |                   |     |     |     |     |     |     |
VIDAK,SNDAK     |                   |____|     |____|     |____|     |____|
                |                   |
                |                   |<t59>|     |<t59>|     |<t59>|     |<t59>|
                |                   |     |<t60>|     |<t60>|     |<t60>|     |
                |                   |  ____     ____      ____      ____|_
RAM Data      _|___________________|/    \___/    \___/    \___/    \
                |                   |\____/   \____/   \____/   \____/
                |                   |
                |                   |<--t61->|                          |
              _|_____________________|_________________________________|__
 ____           |                     \ |                                |
SIRQ            |                      \|_________________________________|__
                |                       |                                |
```

Sym	Parameter	Mes	Nom	Lim	Units	Note
t58	$\overline{VIDRQ}$, $\overline{SNDRQ}$ disable time	25		<120	ns	1
t59	$\overline{VIDAK}$, $\overline{SNDAK}$ pulse width	62	62	> 15	ns	2
t60	$\overline{VIDAK}$, $\overline{SNDAK}$ pulse space	62	62		ns	
t61	$\overline{SNDAK}$ to $\overline{SIRQ}$ active	97	75			3

NOTES:

(1) If $\overline{VIDRQ}$ is not disabled within 120ns of $\overline{VIDAK}$ going LOW, a consecutive Video/Cursor DMA operation will result. Similarly, if $\overline{SNDRQ}$ is not disabled within 120ns of $\overline{SNDAK}$ going LOW, a consecutive Sound DMA operation will result.

(2) The $\overline{VIDAK}$ and $\overline{SNDAK}$ pulse width limits were measured for a sample VIDC. A factor of two should be allowed for process variations.

(3) The $\overline{SIRQ}$ interrupt will be set LOW during sound DMA operations where the *Sound pointer* swaps from the Current to the Next Sound Buffer.

8.8.2 Direct Memory Access - Dynamic RAM read cycles

```
                |                                   |      First        |
                |       Non-sequential access       | Sequential access |
                |                                   |                   |
WE          ___ |___________________________________|___________________|___
(See            |   /                               |                   |
 Note)      ___ |__/                                |                   |
                |                                   |                   |
                |<--- t27 -->|                                    t28 ->|  |<-
            ___ |____________|                                          |  |_
RAS             |            \|                                         |  |/
                |             \_________________________________________|__/__
                |             |                                         |
                |    |<-t29->|  |<- t30                                 |
            ___ |__  |_______|__|_______________  _______________       |
                |  \/     Row    \/    Column 1   \/\/    Column 2   \/\/\/
RA[0:9]     ___ |__/\____________/\_______________/\/\_______________/\/\/\
                |             |    |               |  |               |  |
                |             |    |<t34>|<- t35 ->|  |<t34>|<- t35 ->|  |
                |             |          |                |            |
                |             |<-- t31 ->|<-t32->|<-- t33 ->|<-t32->|
            ___ |____________|_________|        |_________|        |___|__
                |             |         \|       |/        \|       |/  |
CAS[]           |             |          \_______/         \_______/   |
                |             |                                        |
                |             |                                        |
RAM         ___ |____________|____________/           \_______/        |_
Data            |                         \___________/       \_______|_/
                |                                                      |
                |                                                      |
                |<---------- t62 ---------->|<--t59->|<- t60 -->|<-t59->|
            ___ |___________________________|        |__________|       |_
VIDAK,SNDAK                                \|       |/        \|      |/
                |                           \_______/         \_______/
            ->| |    |<- t42                                           |
            ___ |____|_________________________________________________|___
                |   /                                                   |
ROMCS       ___ |__/                                                    |
                |                                                       |
```

NOTE: $\overline{WE}$ is obtained by passing DBE through an external inverter.

Sym	Parameter	Mes	Nom	Lim	Units	Note
t27	$\overline{RAS}$ enable time	110	105		ns	
t28	$\overline{RAS}$ disable time	8	0		ns	
t29	Row Address setup	93	40	> 0	ns	1
t30	Row Address hold	26	20	> 15	ns	1
t31	$\overline{RAS}$ to $\overline{CAS}$[] enable (read)	58	62	> 25	ns	1
t32	$\overline{CAS}$[] pulse width (read)	63	62	> 60	ns	1
t33	$\overline{CAS}$[] precharge period (read)	60	62	> 50	ns	1
t34	Column Address setup (read)	13	20	> 0	ns	1
t35	Column Address hold (read)	89	62	> 20	ns	1
t42	$\overline{ROMCS}$ disable time (DMA cycle)	5	0		ns	
t59	$\overline{VIDAK}$,$\overline{SNDAK}$ pulse width	62	62	> 15	ns	2
t60	$\overline{VIDAK}$,$\overline{SNDAK}$ pulse space	62	62		ns	
t62	$\overline{VIDAK}$,$\overline{SNDAK}$ enable time	188	187		ns	

NOTES:

(1) The DRAM timing limits are given for the particular DRAM used in the test system.

(2) The $\overline{VIDAK}$ and $\overline{SNDAK}$ pulse width limits were measured for a sample VIDC. A factor of two should be allowed for process variations.

8.8.3 Selecting a Video or Cursor DMA

First Video/Cursor DMA request

```
                 ____________
                             \|
VIDRQ                         \____________________________________________
                              |
                     |<t63>|<---------------- t64 ------------------>|
                     |_____________________________________________|
HSYNC    \/\/\/\/                                                   \/\/\/
         /\/\/\/\____________________________________________________/\/\/\
```

Consecutive Video/Cursor DMA requests

```
          |      N-cycle      | S-cycle | S-cycle | S-cycle |
          |                   |         |         |         |
          |                                                   |
VIDRQ  __|___________________________________________________|_
          |                                                   |
          |                                                   |
       __|____________     ____     ____     ____     ____   |_
VIDAK     |            |   |    |   |    |   |    |   |    |
          |            |___|    |___|    |___|    |___|    |
          |                                 |                |
          |                                 |                |
          |                            |<-t65>|<-t66>|        |
          |                            |_____________|        |
HSYNC  \/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
       /\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\/\
          |                                                   |
```

Sym	Parameter	Mes	Nom	Lim	Units	Note
t63	$\overline{HSYNC}$ setup to $\overline{VIDRQ}$ active		20		ns	
t64	$\overline{HSYNC}$ hold from $\overline{VIDRQ}$ active		135		ns	
t65	$\overline{HSYNC}$ setup for consecutive Video/Cursor DMA operations		75		ns	
t66	$\overline{HSYNC}$ hold for consecutive Video/Cursor DMA operations		20		ns	

8.9 I/O Controller Handshaking

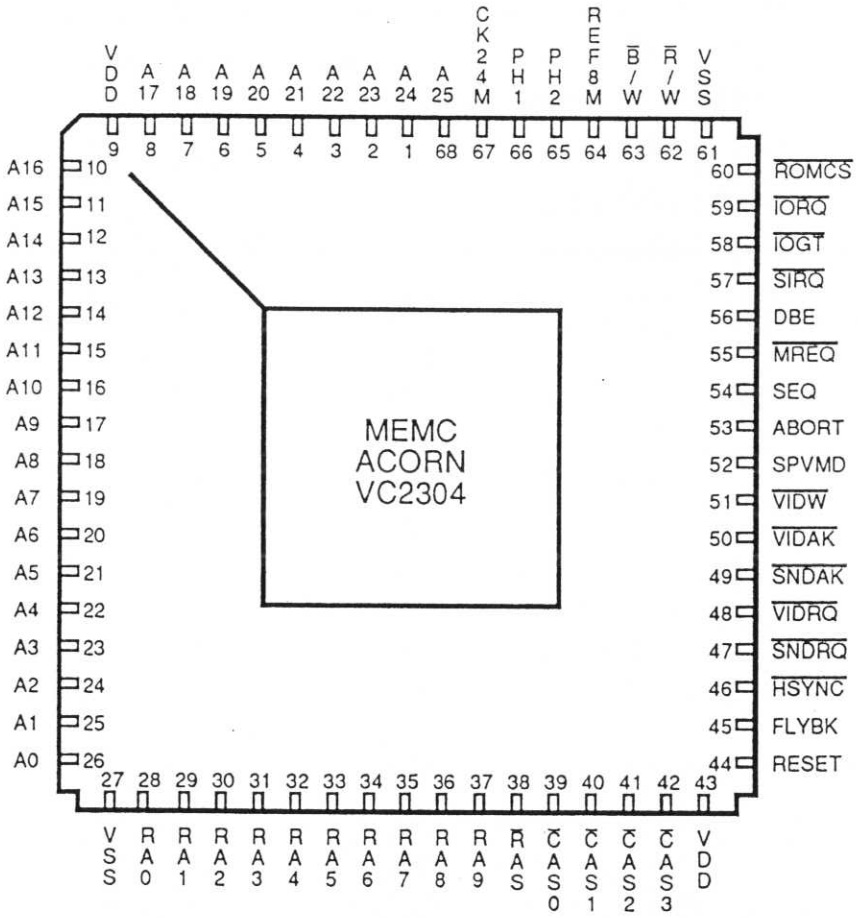
This timing diagram applies when the processor accesses an I/O controller.

```
          __        ____________          ____________
         |  |      |            |        |            |
REF8M    |  |______|            |________|            |____
         |                                            |
         |                 |<------- t67 ------->|<- t69 ->|
         |                 |                     |         |
IORQ     |                \|                     |        /|
(first   |                 \_____________________|_______/ |
 attempt)|                                       |         |
         |                            |<- t68 ->|<- t69 ->|
         |                            |         |         |
IORQ     |                           \|         |        /|
(retries)|                            \_________|_______/ |
         |                                      |         |
         |                                      |         |
         |                          |<t70>|<t71>|         |
         |                          |     |     |         |
IOGT     |                         \/    \/    \/        |
         |                         /\    /\    /\        |
```

Sym	Parameter	Mes	Nom	Lim	Units	Note
t67	$\overline{IORQ}$ setup (first attempt)	110	90		ns	
t68	$\overline{IORQ}$ setup (retries)	62	50		ns	
t69	$\overline{IORQ}$ hold	58	50		ns	
t70	$\overline{IOGT}$ setup		30		ns	
t71	$\overline{IOGT}$ hold		10		ns	

9. Packaging

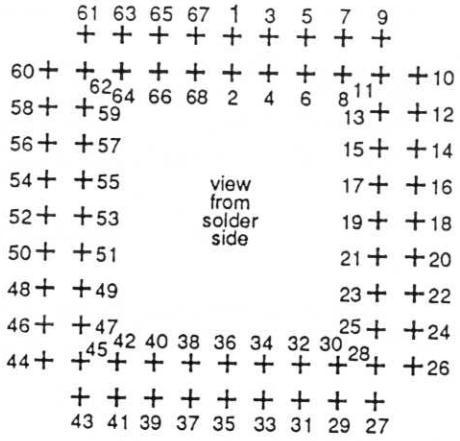
The device is packaged in a JEDEC B ceramic leadless chip carrier, or a JEDEC C plastic leaded chip carrier (PLCC).



Suitable sockets for the devices are:

(i) AMP 55159-1 for the ceramic leadless chip carrier.

(ii) Burndy QILE68P-410T for the plastic leaded chip carrier (PLCC).



Appendix A. RAM address bus

The RAM address bus, **RA[0:9]**, as output from the *DRAM Address Multiplexer* is derived from three sources:

(i) Processor address bus

(ii) Logical to Physical Address Translator

(iii) DMA Address Generators

During processor accesses to Physically mapped RAM, the higher order bits of the address bus, **A[2:25]**, define the Physical page to be accessed, and the lower order bits define the word offset within that page. Similarly, when the processor accesses Logically mapped RAM, the *Logical to Physical Address Translator* supplies the Physical page number (provided that the access is successful). The row and column addresses supplied to the DRAM on **RA[0:9]** during processor accesses are a combination of the Physical page number (*PPN[0:6]*) and word offset (**A[2:14]**).

During DMA operations, the *DMA Address Generators* supply a 17-bit word address from which data is to be fetched. The DMA address is strobed to the DRAMs as a row and column address. The DMA Address Generators can only address 512kBytes, so the top bits of the address strobed to the DRAMs are padded with zeros to force the access in the bottom 512KBytes of memory.

Refresh operations use the address supplied by the *Video pointer* register in the DMA Address Generators.

The values output on the RAM address bus depend upon the Page size selected. Figure 13 shows the signal seen on **RA[0:9]** for each of the four Page sizes.

NOTES:

(i) The outputs of the DRAM Address Multiplexer pass through inverting pads, so the signals seen on **RA[0:9]** are inverted.

(ii) **A[2:14]** are 13-bits of the processor address bus that define the word offset within a Physical page.

(iii) *PPN[0:6]* are 7-bits that define the Physical page number being accessed.

(iv) *DMA[2:18]* are 17-bits from the DMA Address Generators that define the physical word address of a DMA read operation.

4KByte Page Size

RAM address bus

		RA[9]	RA[8]	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
Processor access	Row address	X	X	$\overline{A}$[11]	$\overline{A}$[10]	$\overline{A}$[9]	$\overline{A}$[8]	$\overline{A}$[7]	$\overline{A}$[6]	$\overline{A}$[5]	$\overline{A}$[4]
	Column address	X	$\overline{PPN}$[6]	$\overline{PPN}$[5]	$\overline{PPN}$[4]	$\overline{PPN}$[3]	$\overline{PPN}$[2]	$\overline{PPN}$[1]	$\overline{PPN}$[0]	$\overline{A}$[3]	$\overline{A}$[2]
DMA and refresh operations	Row address	X	X	$\overline{DMA}$[11]	$\overline{DMA}$[10]	$\overline{DMA}$[9]	$\overline{DMA}$[8]	$\overline{DMA}$[7]	$\overline{DMA}$[6]	$\overline{DMA}$[5]	$\overline{DMA}$[4]
	Column address	X	$\overline{DMA}$[18]	$\overline{DMA}$[17]	$\overline{DMA}$[16]	$\overline{DMA}$[15]	$\overline{DMA}$[14]	$\overline{DMA}$[13]	$\overline{DMA}$[12]	$\overline{DMA}$[3]	$\overline{DMA}$[2]

8KByte Page Size

RAM address bus

		RA[9]	RA[8]	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
Processor access	Row address	X	$\overline{A}$[12]	$\overline{A}$[11]	$\overline{A}$[10]	$\overline{A}$[9]	$\overline{A}$[8]	$\overline{A}$[7]	$\overline{A}$[6]	$\overline{A}$[5]	$\overline{A}$[4]
	Column address	X	$\overline{PPN}$[5]	$\overline{PPN}$[4]	$\overline{PPN}$[3]	$\overline{PPN}$[2]	$\overline{PPN}$[1]	$\overline{PPN}$[0]	$\overline{PPN}$[6]	$\overline{A}$[3]	$\overline{A}$[2]
DMA and refresh operations	Row address	X	$\overline{DMA}$[12]	$\overline{DMA}$[11]	$\overline{DMA}$[10]	$\overline{DMA}$[9]	$\overline{DMA}$[8]	$\overline{DMA}$[7]	$\overline{DMA}$[6]	$\overline{DMA}$[5]	$\overline{DMA}$[4]
	Column address	X	$\overline{DMA}$[18]	$\overline{DMA}$[17]	$\overline{DMA}$[16]	$\overline{DMA}$[15]	$\overline{DMA}$[14]	$\overline{DMA}$[13]	1	$\overline{DMA}$[3]	$\overline{DMA}$[2]

16KByte Page Size

RAM address bus

		RA[9]	RA[8]	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
Processor access	Row address	X	$\overline{A}$[12]	$\overline{A}$[11]	$\overline{A}$[10]	$\overline{A}$[9]	$\overline{A}$[8]	$\overline{A}$[7]	$\overline{A}$[6]	$\overline{A}$[5]	$\overline{A}$[4]
	Column address	$\overline{PPN}$[6]	$\overline{PPN}$[4]	$\overline{PPN}$[3]	$\overline{PPN}$[2]	$\overline{PPN}$[1]	$\overline{PPN}$[0]	$\overline{A}$[13]	$\overline{PPN}$[5]	$\overline{A}$[3]	$\overline{A}$[2]
DMA and refresh operations	Row address	X	$\overline{DMA}$[12]	$\overline{DMA}$[11]	$\overline{DMA}$[10]	$\overline{DMA}$[9]	$\overline{DMA}$[8]	$\overline{DMA}$[7]	$\overline{DMA}$[6]	$\overline{DMA}$[5]	$\overline{DMA}$[4]
	Column address	1	$\overline{DMA}$[18]	$\overline{DMA}$[17]	$\overline{DMA}$[16]	$\overline{DMA}$[15]	$\overline{DMA}$[14]	$\overline{DMA}$[13]	1	$\overline{DMA}$[3]	$\overline{DMA}$[2]

32KByte Page Size

RAM address bus

		RA[9]	RA[8]	RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
Processor access	Row address	$\overline{A}$[13]	$\overline{A}$[12]	$\overline{A}$[11]	$\overline{A}$[10]	$\overline{A}$[9]	$\overline{A}$[8]	$\overline{A}$[7]	$\overline{A}$[6]	$\overline{A}$[5]	$\overline{A}$[4]
	Column address	$\overline{PPN}$[5]	$\overline{PPN}$[3]	$\overline{PPN}$[2]	$\overline{PPN}$[1]	$\overline{PPN}$[0]	$\overline{A}$[14]	$\overline{PPN}$[6]	$\overline{PPN}$[4]	$\overline{A}$[3]	$\overline{A}$[2]
DMA and refresh operations	Row address	$\overline{DMA}$[13]	$\overline{DMA}$[12]	$\overline{DMA}$[11]	$\overline{DMA}$[10]	$\overline{DMA}$[9]	$\overline{DMA}$[8]	$\overline{DMA}$[7]	$\overline{DMA}$[6]	$\overline{DMA}$[5]	$\overline{DMA}$[4]
	Column address	1	$\overline{DMA}$[18]	$\overline{DMA}$[17]	$\overline{DMA}$[16]	$\overline{DMA}$[15]	$\overline{DMA}$[14]	1	1	$\overline{DMA}$[3]	$\overline{DMA}$[2]

Figure 13: RAM address bus signals